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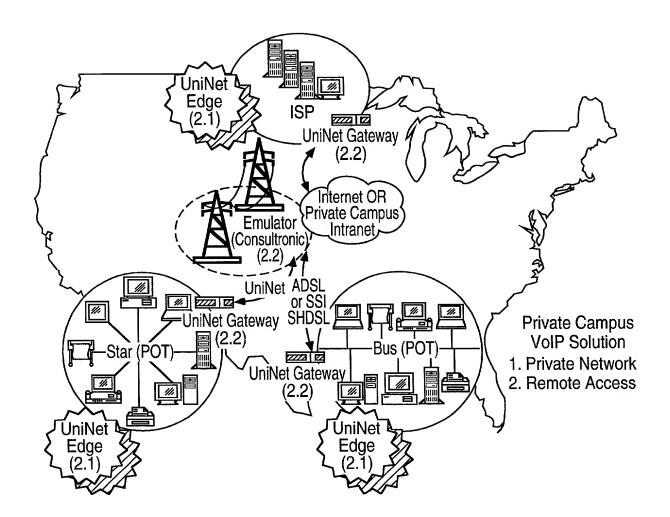
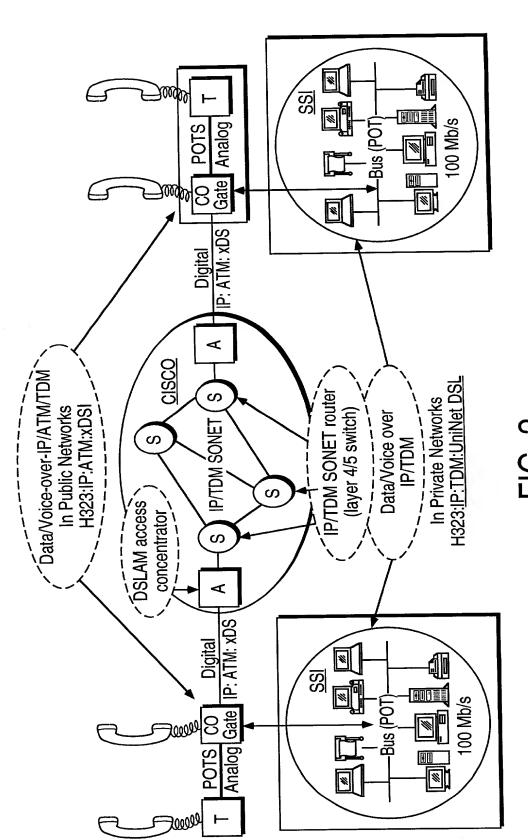


FIG. 1 Universal Intelligence Network (UniNet"™)

Title: "Channel Equalization System And Method" Inventors: Francois Trans & Tho Le-Ngoc Atty. Docket No.: 20870-06001; Case 6001 US Application No.: Not Yet Known Sheet 2 of 97



Private UniNetTM Networks FIG. 2

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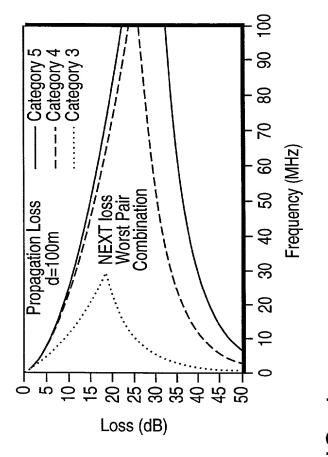
Title: "Channel Equalization System And Method" Inventors: Francois Trans & Tho Le-Ngoc Atty. Docket No.: 20870-06001; Case 6001 US Application No.: Not Yet Known Sheet 3 of 97

node 1 node 2 node 3 node 4 bus A bus B

FIG. 3 UniNet nodes interconnected in a mesh structure

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Cable

 $V_{S(t)}$

Pair

Pair

FIG. 4

Typical Near End and Far End Cross-talks Noise Environment

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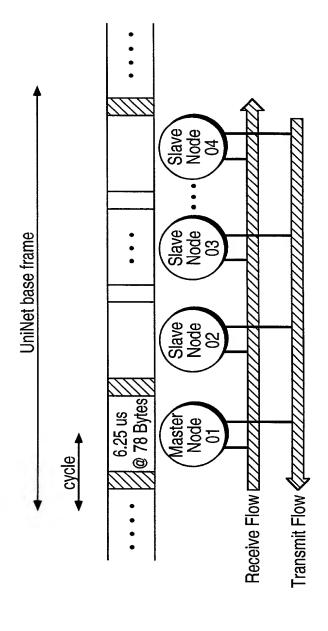


FIG. 5

TDM Transmit and Receive Flow cycles

The state of the s

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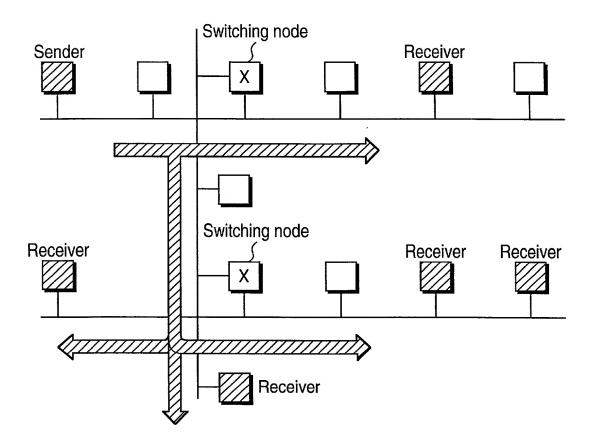


FIG. 6
A UniNet Multicast Group

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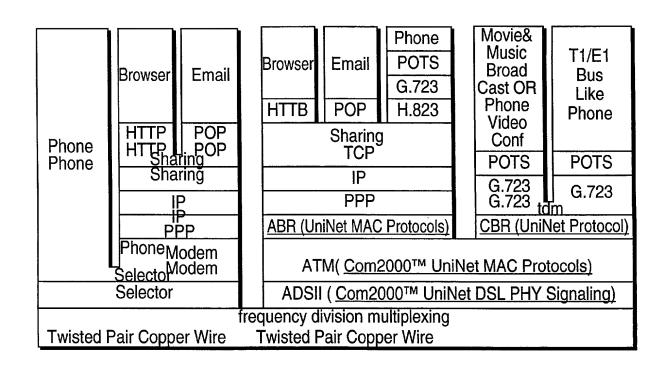


FIG. 7
UniNet Network over Plain Old Telephone Systems (POTS)

Title: "Channel Equalization System And Method"

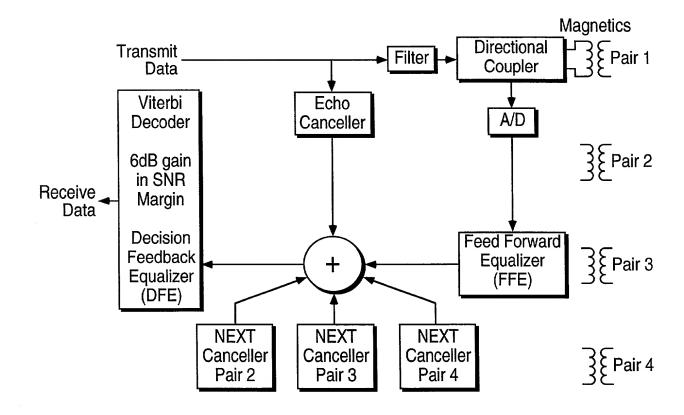


FIG. 8 Typical Parallel Channels for ECHO, NEXT and FEXT Cancellations

The state of the

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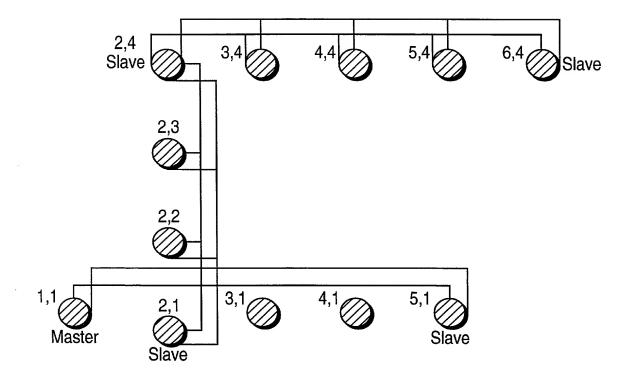


FIG. 9
UniNet Hierarchical Synchronization

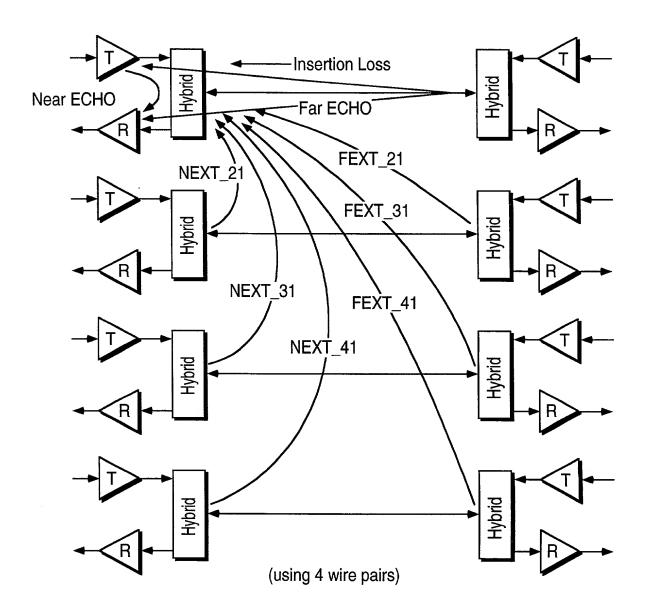


FIG. 10 Gigabit Ethernet over 4 pairs of UTP cables

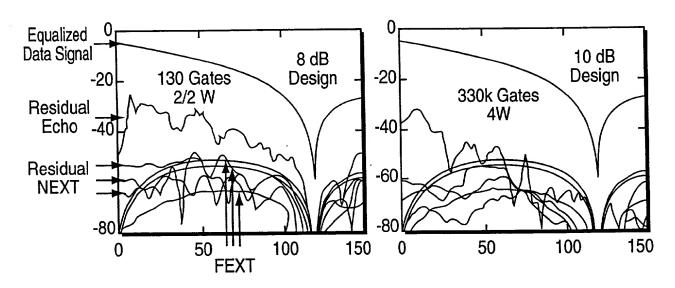


FIG. 11A

	3 dB Design	10 dB Design
Margin without FEXT	3.5 dB	10.7 dB
Margin with FEXT	2.5 dB	6.7 dB
Margin with FEXT + 3	1.8 dB	4.9 dB

FIG. 11B

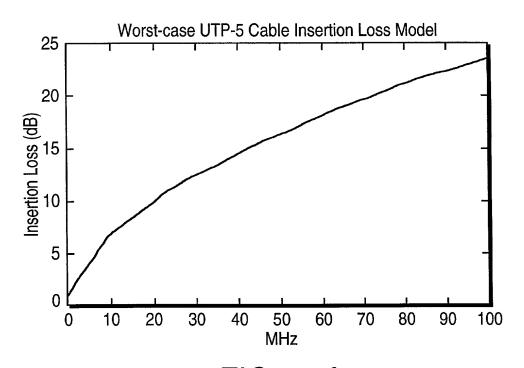
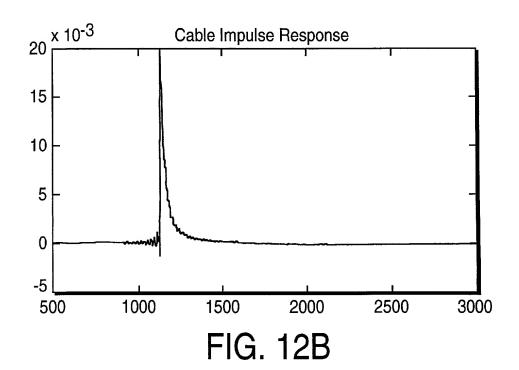
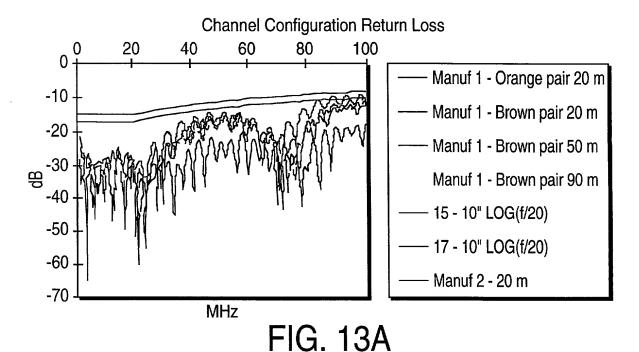


FIG. 12A
Worst-case Insertion Loss of 100m, cat-5 Cable



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Overall Return Loss of Different Cable Channel

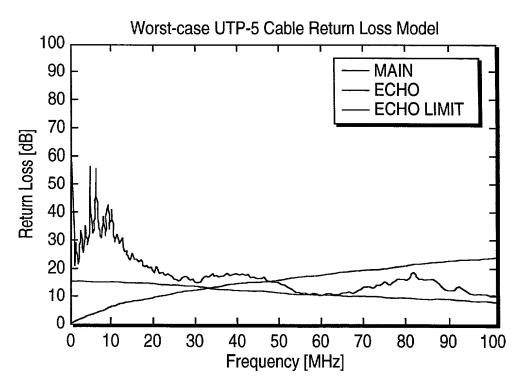


FIG. 13B
Worst Case Return Loss Relative to Main Signal

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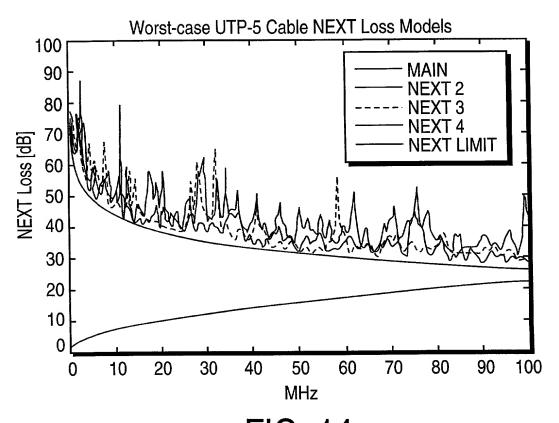


FIG. 14
NEXT loss between pairs of cat-5 cables

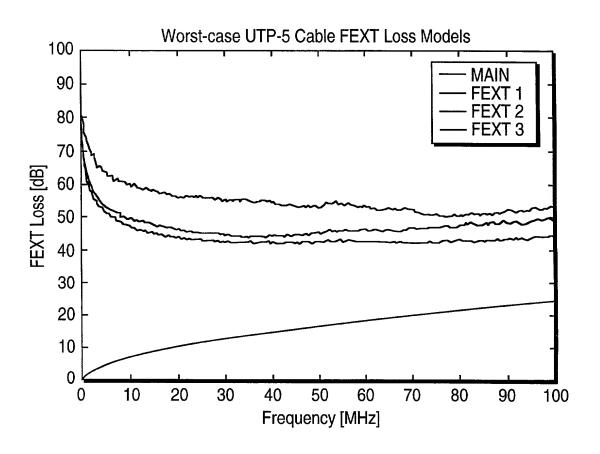


FIG. 15
FEXT Loss Characteristics

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 $\{1+(\omega/\omega_{\rm C})^2\}^{-1}$ $\{1+(\omega/\omega_{\rm C})^2\}^{-1}$ $0.75 + 0.25z^{-1}$ $\{1+(\omega/\omega_{\rm C})^{2}\}^{-1}$ $\{1+(\omega/\omega_{\rm C})^2\}^{-1}$ 0.75+0.25z⁻¹ $\{1+(\omega/\omega_{\rm C})^{2}\}^{-1}$ $\{1+(\omega/\omega_{\rm C})^2\}^{-1}$ 0.75+0.25z⁻¹ $N_2(\omega)$ **AWN** $\{1+(\omega/\omega_{\rm C})^2\}^{-1}$ $\{1+(\omega/\omega_{\rm C})^2\}^{-1}$ 0.75+0.25z⁻¹ $N_3(\omega)$ $\{1+(\omega/\omega_{\rm C})^2\}^{-1}$ $\{1+(\omega/\omega_{\rm C})^{2}\}$ 0.75+0.25z⁻¹ $\{1+(\omega/\omega_{\rm C})^{10}\}^{-1}$ Receiver

FIG. 16
System Modeling

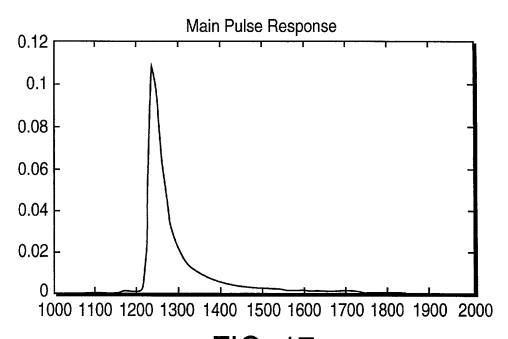
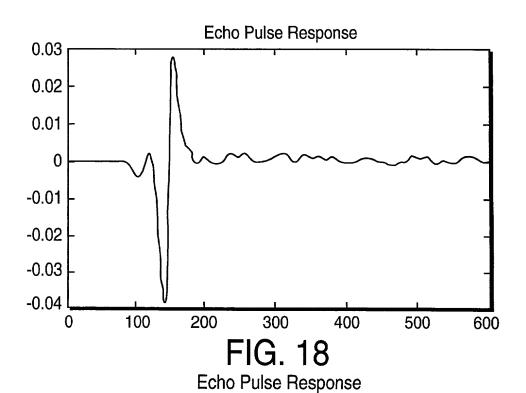


FIG. 17 Received (desired) pulse response



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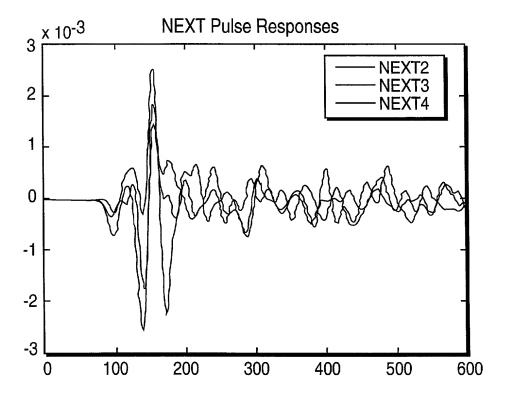


FIG. 19A

NEXT Pulse Responses

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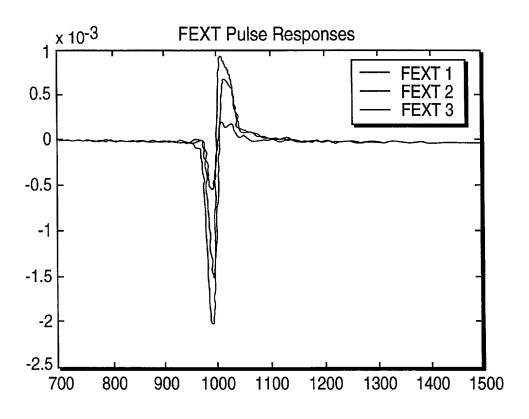
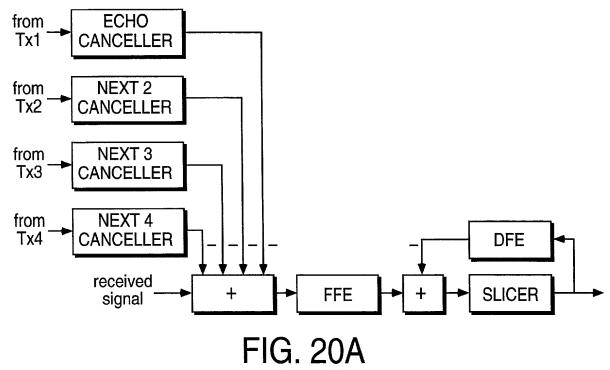


FIG. 19B
NEXT Pulse Responses

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Receiver Structure Using Interference Cancellers Prior to Equalizers

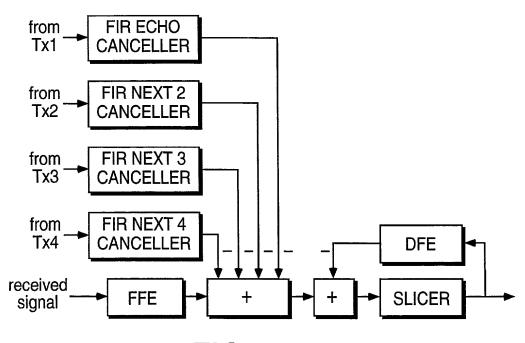


FIG. 20B

Receiver Using Interference Cancellers After FFE

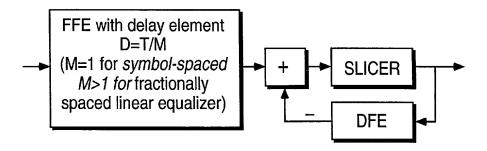
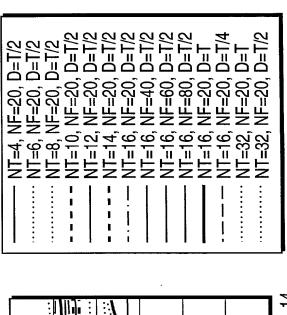
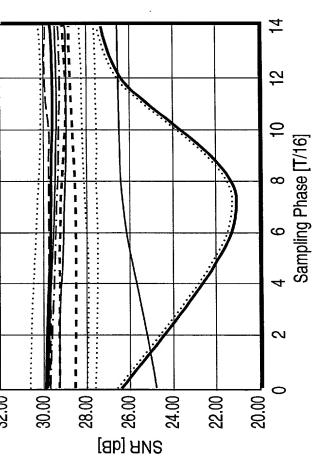


FIG. 20C

Receiver using cascaded FSLE/DFE for both interference suppression and equalization

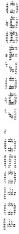
Title: "Channel Equalization System And Method" Inventors: Francois Trans & Tho Le-Ngoc Atty Docket No.. 20870-06001; Case 6001 US Application No.: Not Yet Known Sheet 22 of 97

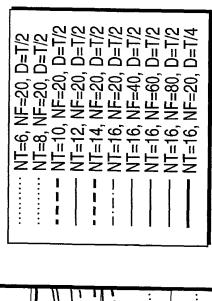




-IG. 21

SNR versus Sampling Phase of different FFE/DFE configurations





30.00-

29.00-

SNR [qB]

28.00

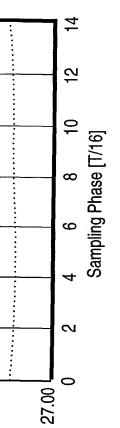
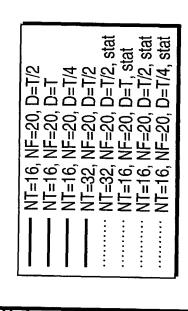


FIG. 22 SNR versus Sampling Phase for various FSLE/DFE configurations



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24.00-

30.00

32.00

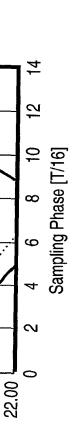


FIG. 23 SNR vs Sampling Phase

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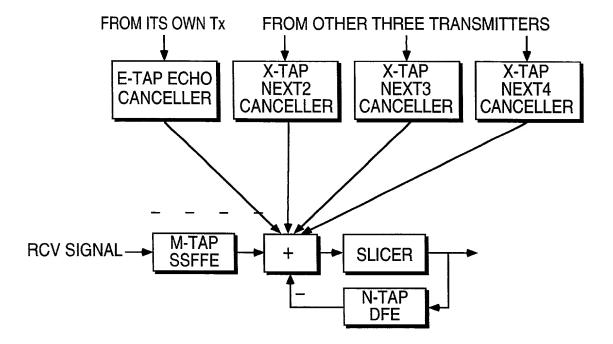


FIG. 24 **Currently Proposed Structure**

MARGIN [dB] OFFERED BY DIFFERENT SCHEMES

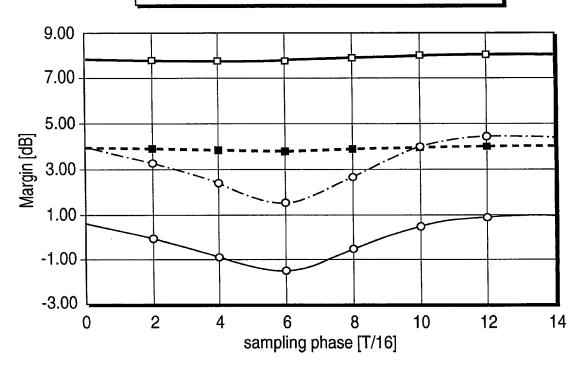
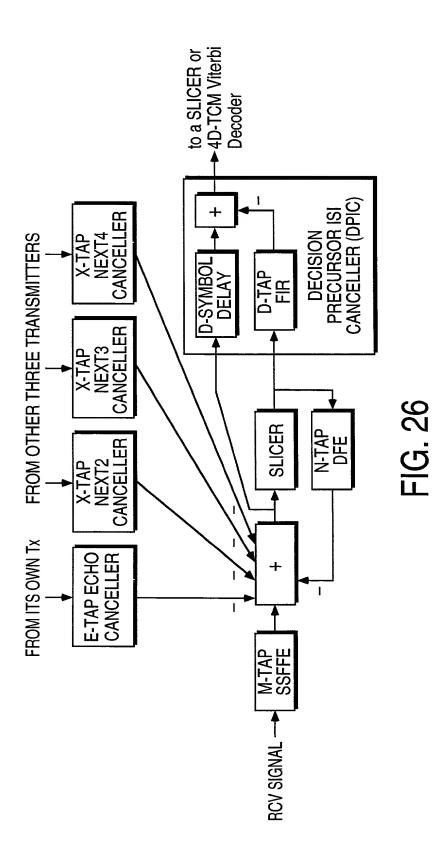


FIG. 25
Margin Offered by Different Schemes

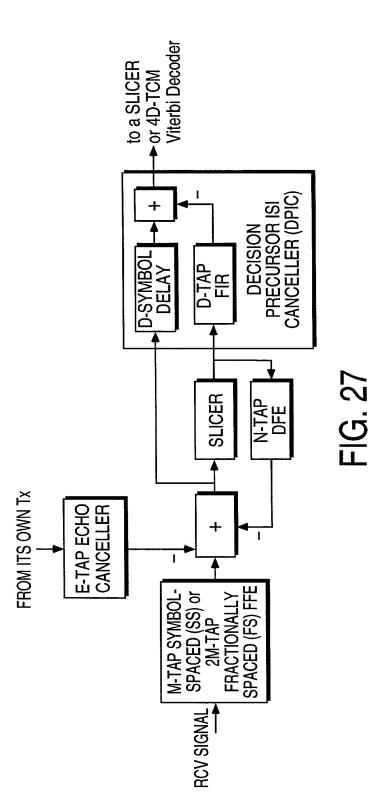
Title: "Channel Equalization System And Method" Inventors: Francois Trans & Tho Le-Ngoc Atty. Docket No.: 20870-06001; Case 6001 US Application No.: Not Yet Known Sheet 27 of 97



Improved-Performance Receiver Structure

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Receiver Structure using DPIC without NEXT cancellers

12:

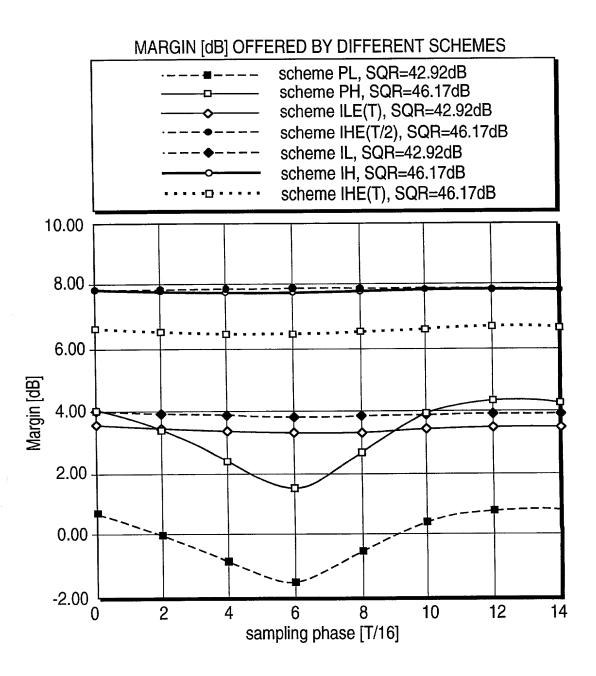


FIG. 28
Margin Offered by Various Schemes

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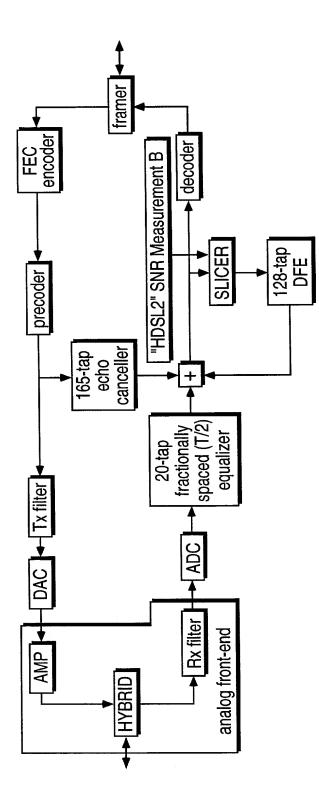


FIG. 29
Existing SHDSL Transceiver Structure

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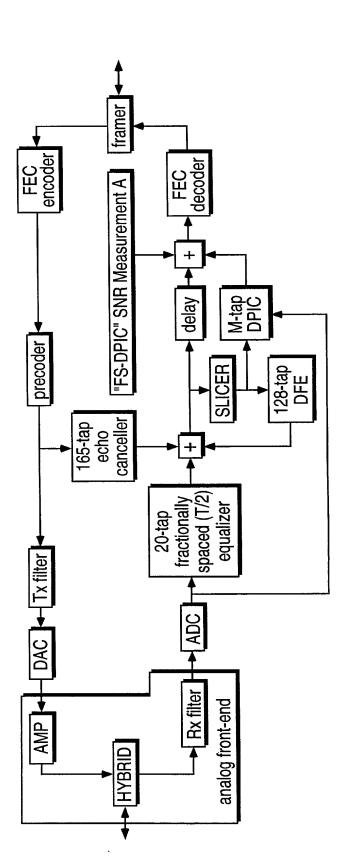
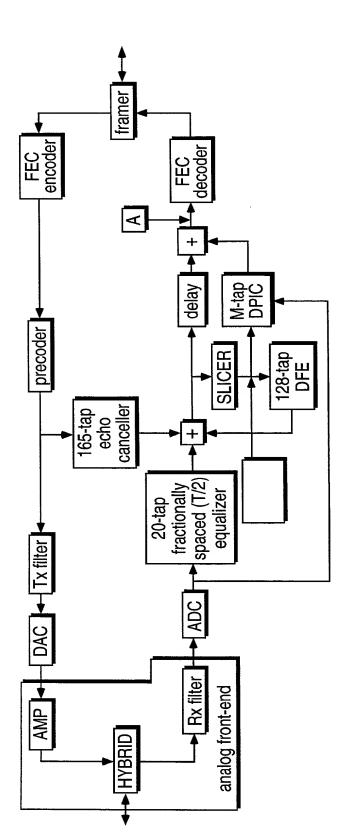


FIG. 30 Proposed Transceiver Structure using DPIC

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SNR Measurement Points (A,B) (Proposed Transceiver Structure using DPIC) FIG. 31

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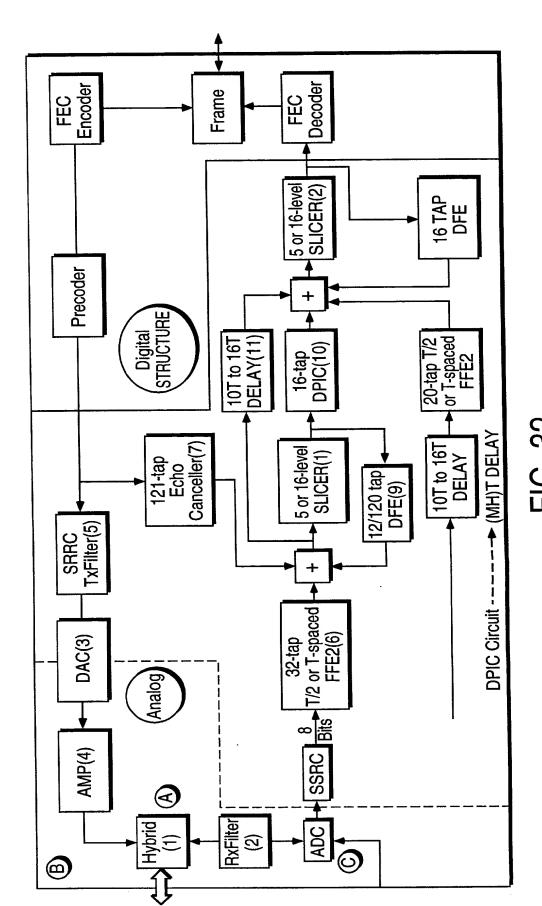


FIG.~32 HDSL2 Front-End (Converter & Sampler & Equalizers)

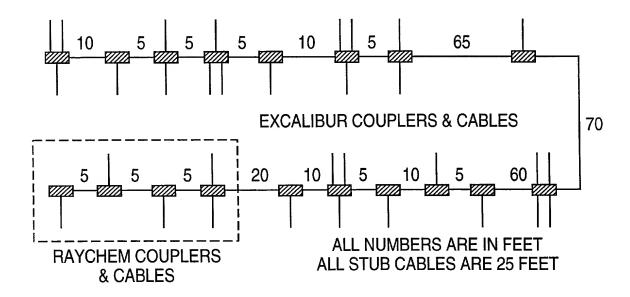


FIG. 33A
SAE Developed De Long Network

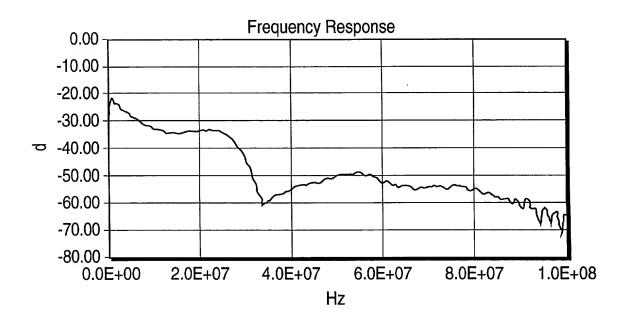


FIG. 33B
SAE Developed De Long Network Impulse Response

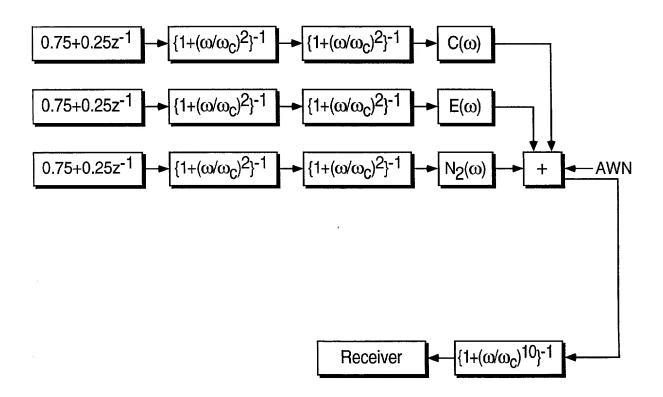
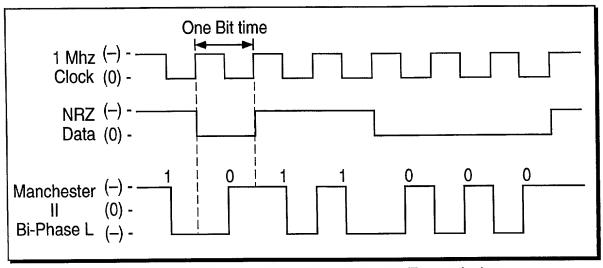


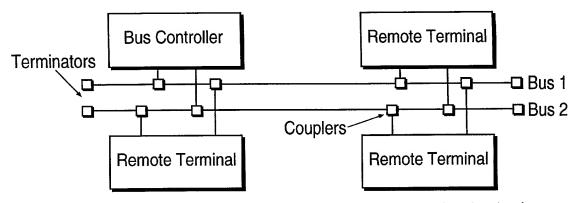
FIG. 34
Next Generation 1553 System Modeling

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FIG. 35
Current 1553 Architecture and Data Coding Scheme



Data Coding Scheme of Current 1553 Data Transmissions



Example of Current 1553 Bus Cabling Architecture (Redundant)

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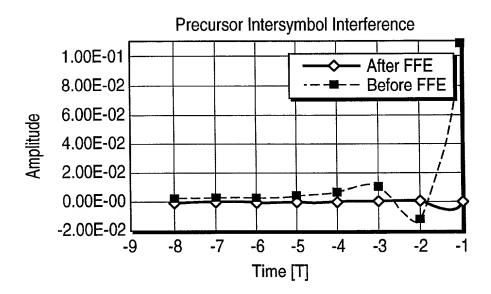
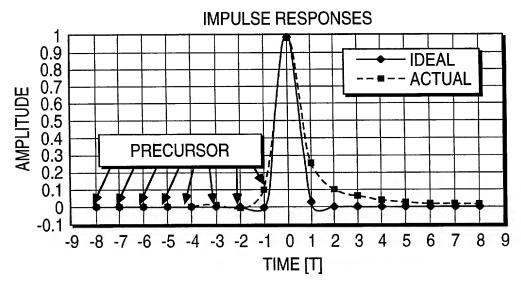


FIG. 36

Before and After Fractional Space Equalizer for Precursor ISI

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100Mb/s USING PAM 8 over a 100m-cable

FIG. 37
Intersymbol Interference (ISI) at High
Transmission Rate Over MIL-C17 Cable

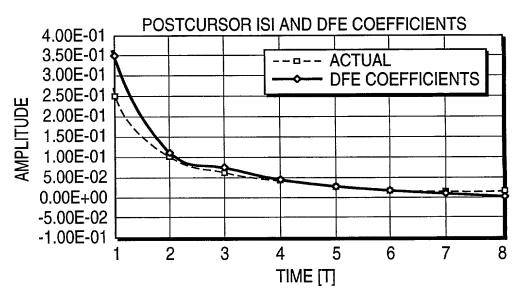


FIG. 38

Decision Feedback Equalization to Remove Postcursor ISI

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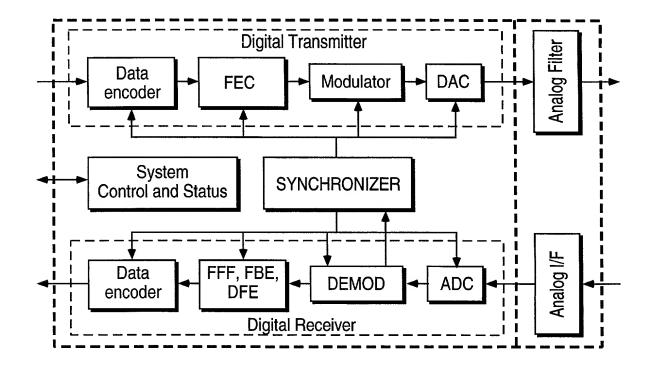
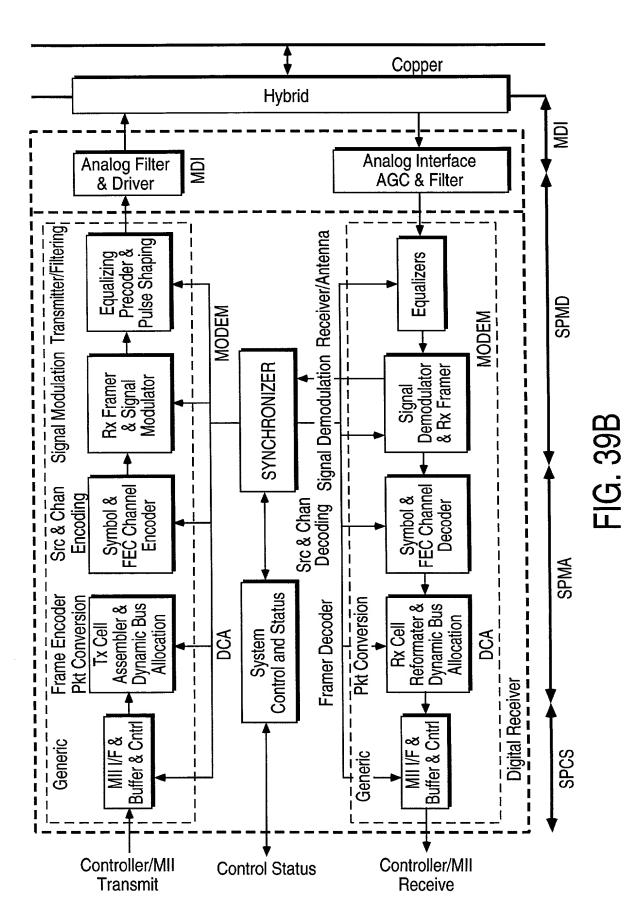


FIG. 39A
Proposed High Level 1553+ Transceiver Structure High Level

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Proposed Medium Level 100Mb/s1553+ Transceiver Structure High Level

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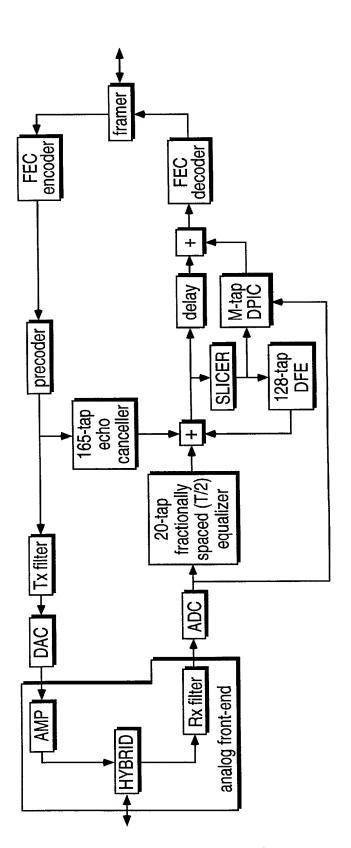


FIG. 39C
Proposed Detailed 100Mb/s 1553+ Transceiver Structure using DPIC

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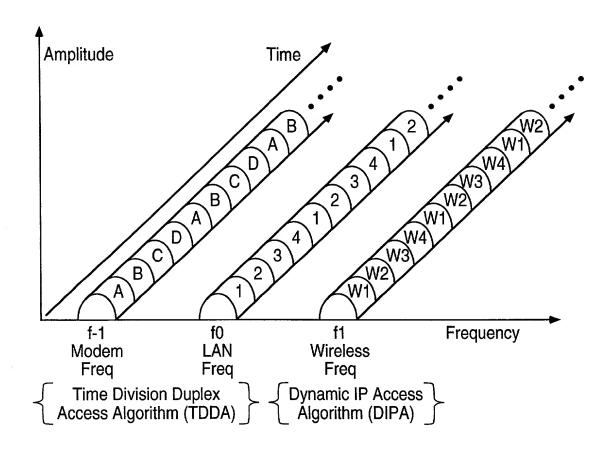


FIG. 40 Channelization/Timer Division Multiplex Access (TDMA/TDD)

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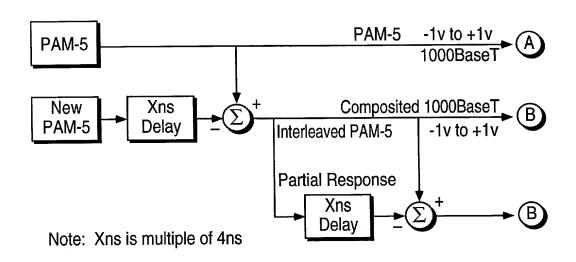
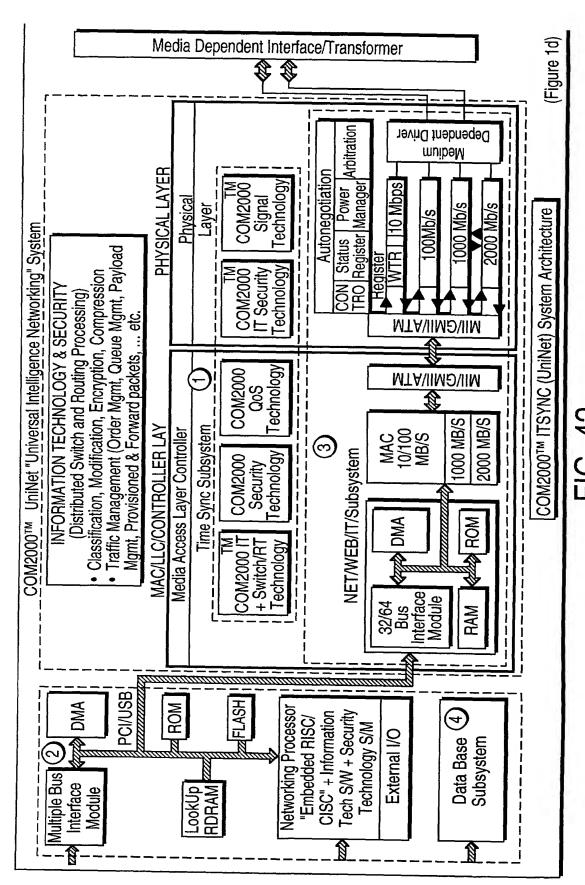
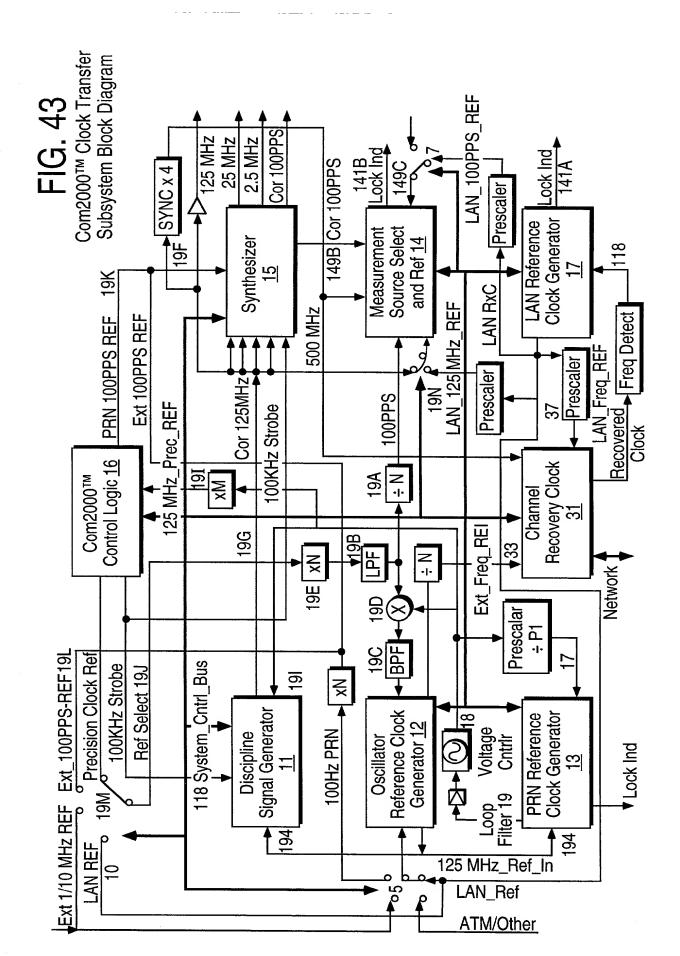


FIG. 41
Com2000™ PAM-5 Partial Response Signaling Overview

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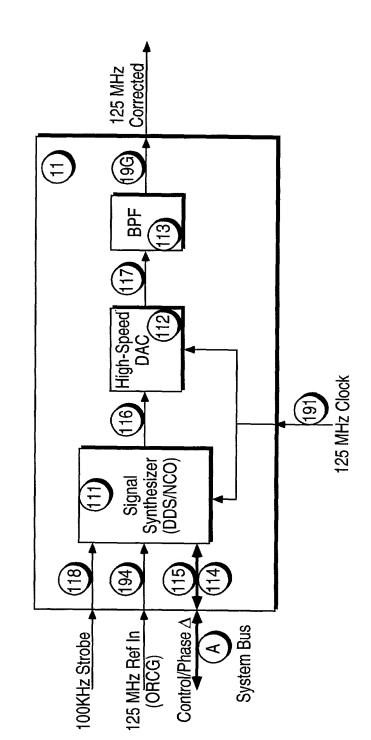


UniNet Internet Communication Processor FIG. 42



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FIG. 43A
Discipline Signal Generator



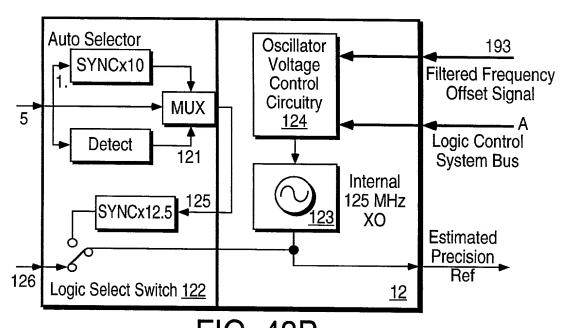


FIG. 43B
Oscillator Reference Clock Generator

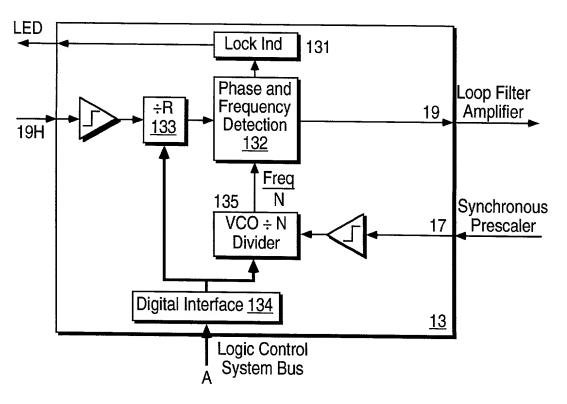
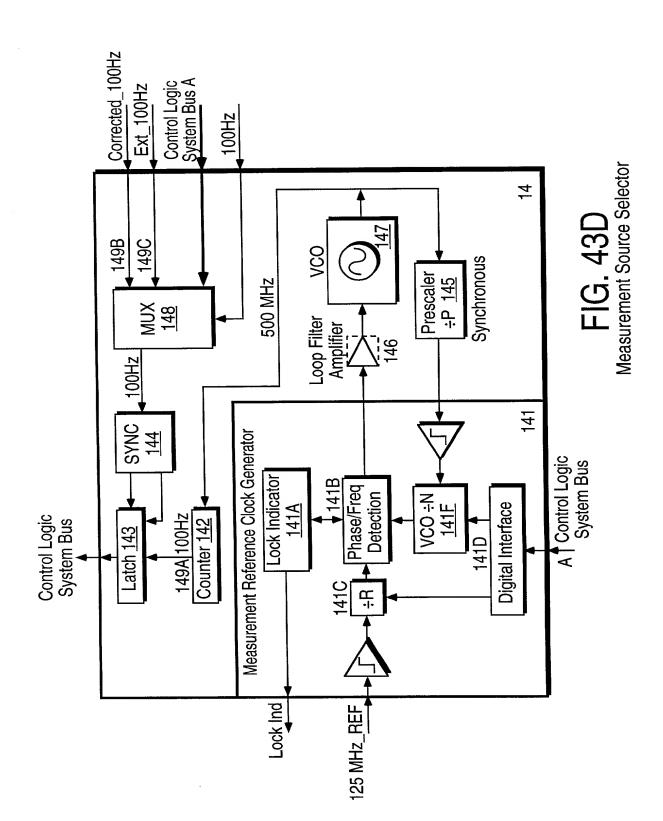
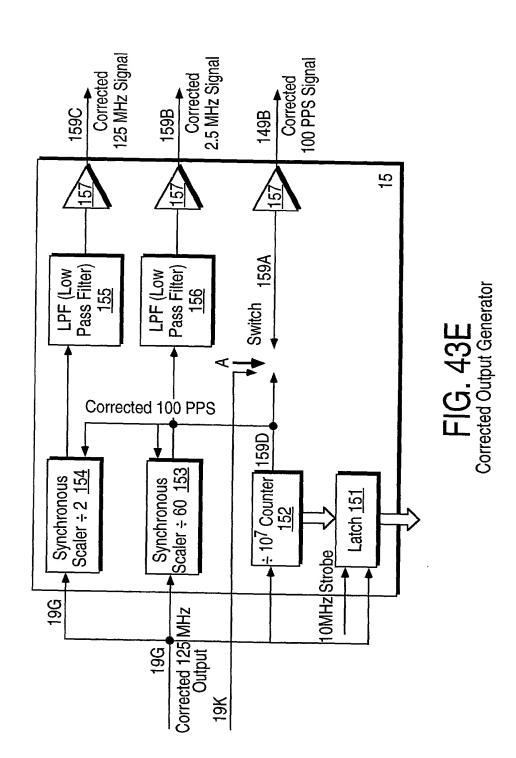


FIG. 43C
Precision Reference Clock Generator

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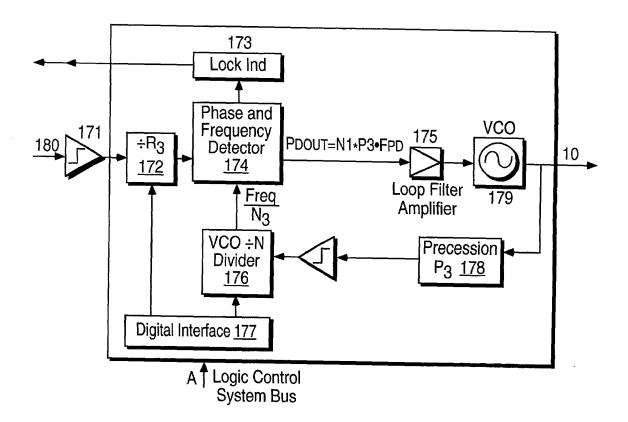


FIG. 43F Com REF Clock Generator

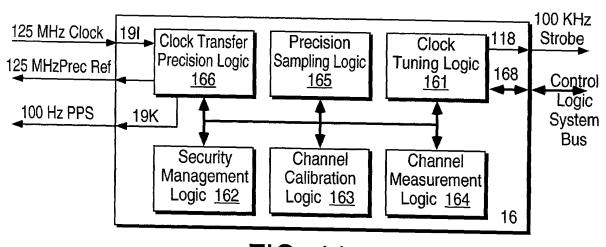
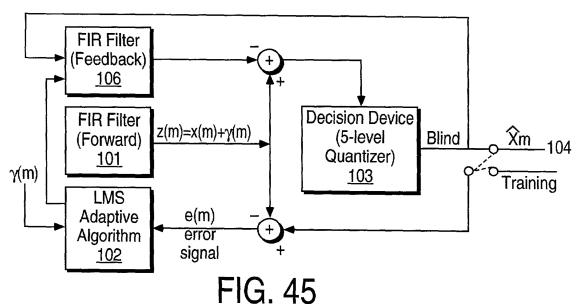


FIG. 44 Com 2000™ Clock Transfer Control Logic



Com2000™ LMS Adaptive Equalizer

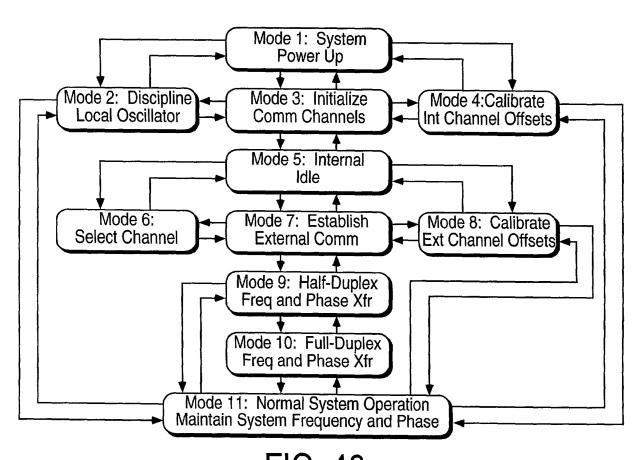
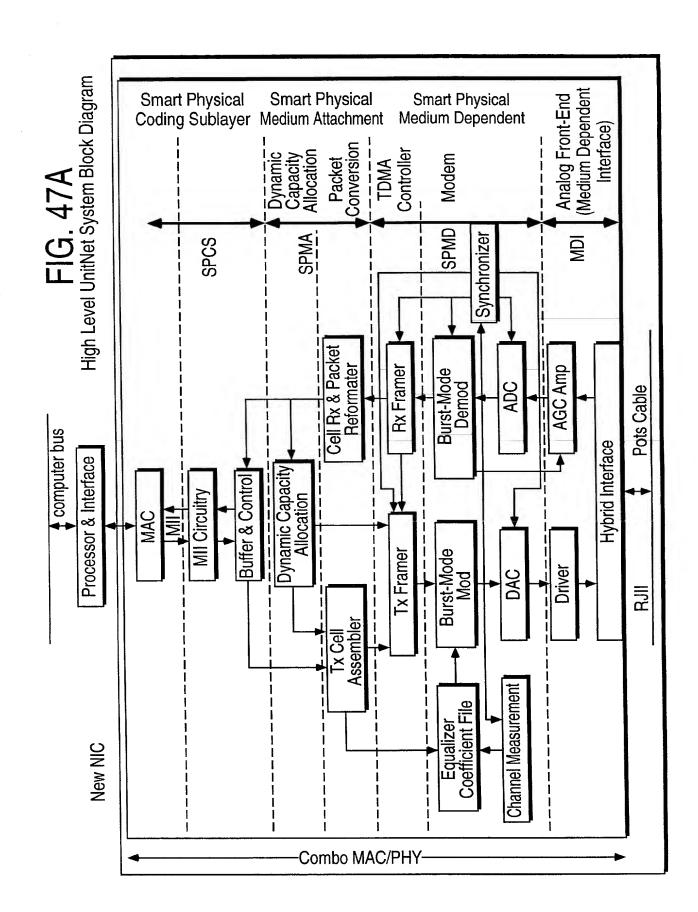
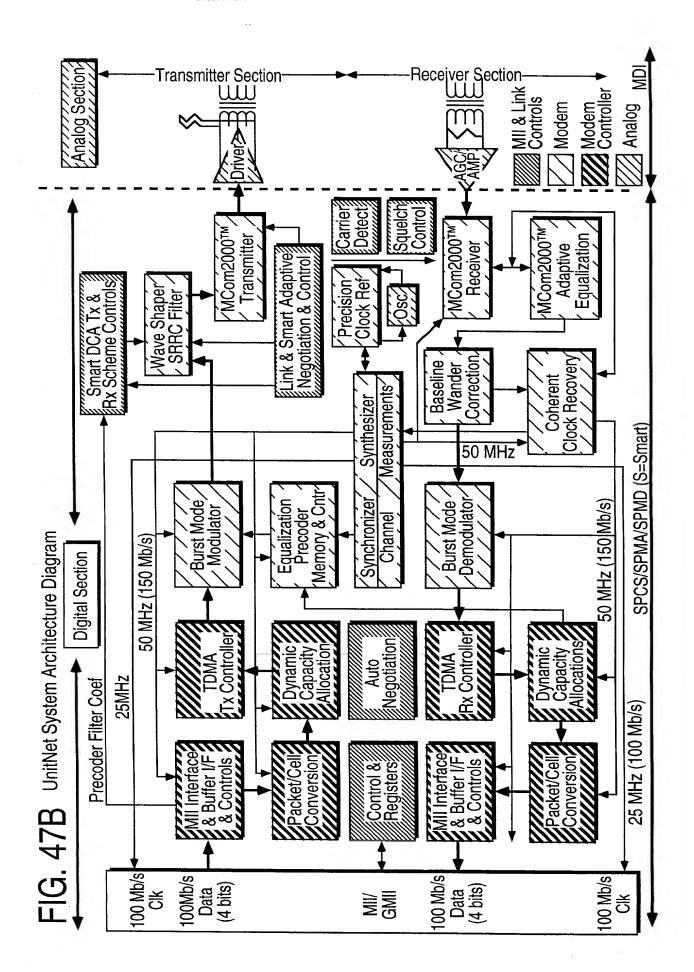


FIG. 46
Com 2000™ State Transition Diagram

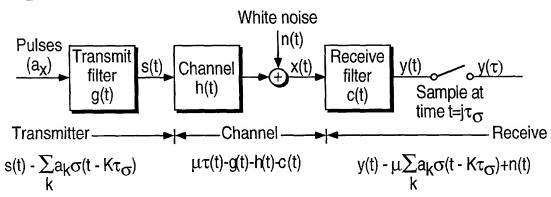




Generic Tuning M201 Algorithm M216 Suspend For Time **Received Derived** Δ Time & Δ Freq. M202 M215 Offset Values Perform Frequency Jam M203 1s ∆f< No 500ps/s? ,Yes Adjust Frequency M204 Jam Gain M205 Is ∆f< No 50ps/s? Frequency Tuning Yes Cycle M206 M214 Adjust Gain & Perform Is $\Delta f <$ No 20ps/s? Frequency Fine Tuning Perform Yes Phase Jam M207 ls ∆T< No M213 100ns? Yes **Adjust Phase** Phase M208 Jam Gain Tuning Cycle M209 Îs ∆T< No 50ns? M211 ŢYes M210 M212 Data Valid Adjust Fine Perform Phase OK On Phase Tune Gain Fine Tuning Disciplined

FIG. 48
Generic Tuning Algorithm

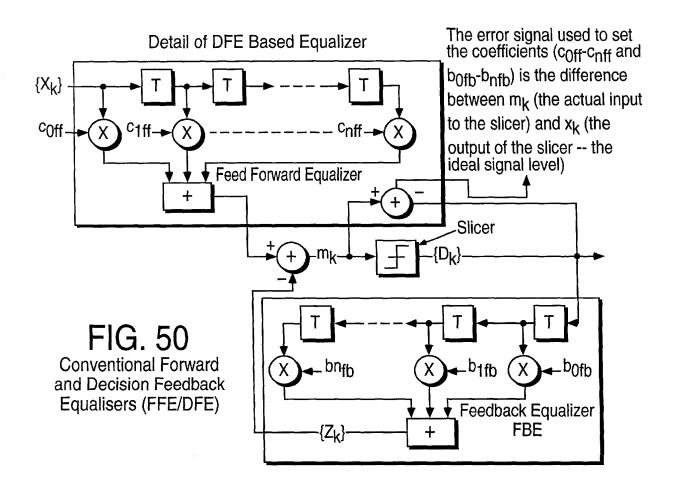
Intersymbol Interference



The receiver filter output is sampled at time intervals ta=trb giving

$$y(t_1) - \sum_{k=0}^{\infty} P((t-K)T_0) + n(t_1)$$

$$FIG. 49 - \mu \alpha_t + \mu \sum_{k=0}^{\infty} a_k P((i-K)T_0) + n(t_1)$$
 The ISI Definitions



(20*6.25 us or 10 nodes in the UniNet network), as shown in figure 05

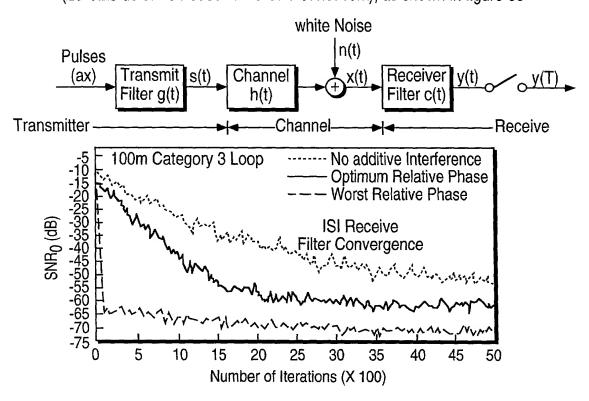


FIG. 51A

Phase Dependent Convergence of a FFE/DFE Filter

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Performance of 51.84 Mb/s 16-CAP transceiver over 100 m category 3 cable with one cyclostationary NEXT interferes

TIA/EIA NEX	XTR model	a = 1.2	1/T =	12.96 Mbauch	$P_2 = 10^{-10^*}$	
φ1	SNRi	SN	R ₁ SNR _n		Margin	
(i T/δ)	(dB)	(dB)		(dB)	(dB)	
φ0	12.5	13	.0	54.9	31.65	
φ1	12.5	14	.8	58.1	43.85	
φ2	12.5	18	.3	61.3	38.05	
φз	12.5	18	.4	61.9	38.65	
φ4	12.5	14	.8	60.5	37.35	
φ5	12.5	13.0		57.1	33.85	

^{*}Margins are with respect to $P_2 = 10^{-10}$ for which $SNR_{0,mf} = 23.23$ dB

FIG. 51B Phase Dependent Convergence of FFE/DFE Filter - SNR

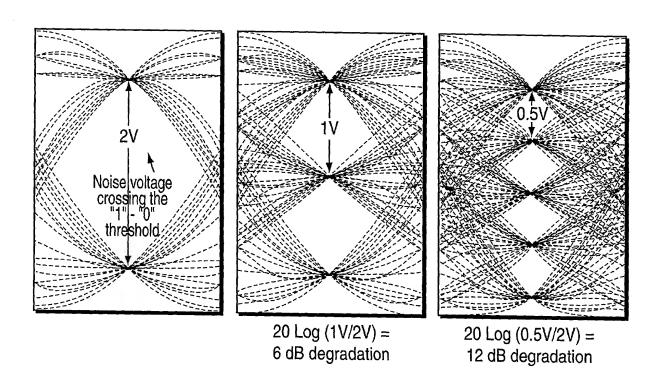


FIG. 52A
The Eye Open Diagram of Biphase Manchester, MLT3 and PAM5

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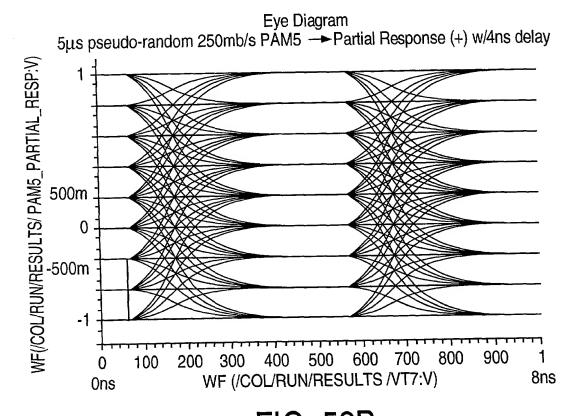


FIG. 52B
The Signal Spectrum and Eye Open Diagram of SPAM5

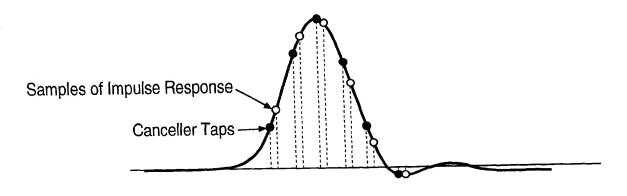


FIG. 53
The ECHO and NEXT Canceller Filter Performance

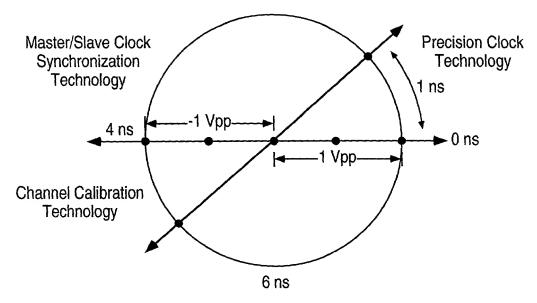
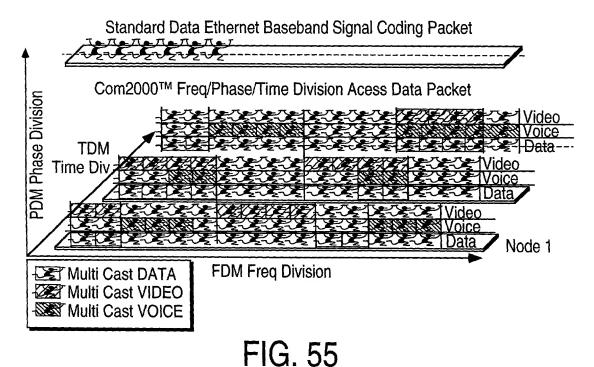
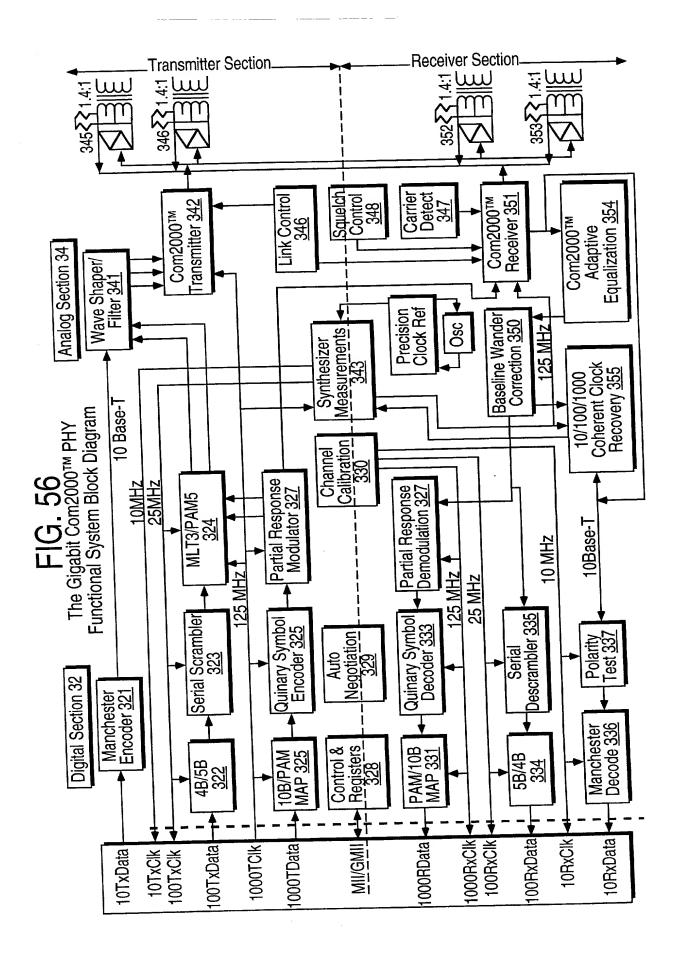


FIG. 54
Precision Phase Angle Controls



Time, Phase, Frequency Division Multiple Access Signal Coding Scheme



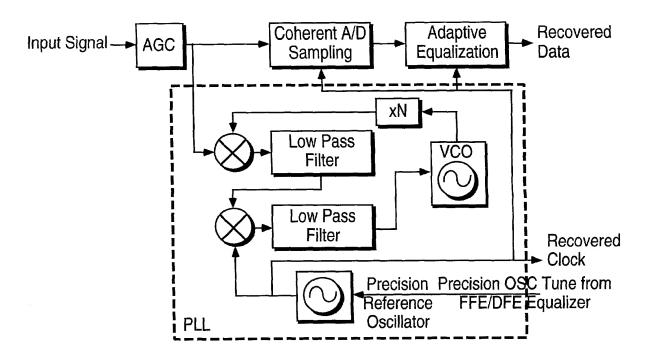
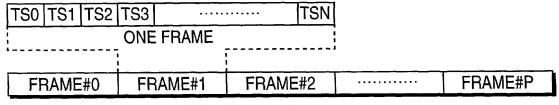


FIG. 57
Coherent Carrier Recover PLL Loop for UniNet Receiver



ONE MULTIFRAME (optional)

FIG. 58
General Frame Structures

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TS0	TS1	TS2	TS3	••••	TSj	Empty Zone nTS	TSk	TS(k+1)		TSN
DOWNSTREAM SECTION						UPSTREAM SECTION				
ONE FRAME										

FIG. 59
Downstream and Upstream Sections

TIME-SLOT						
PRE-AMBLE		CELL				
G (g bits)	UW (u bits)	T (t bits)	H (h bits)	PAYLOAD (p bits)		

FIG. 60 Simplified Burst and Cell Structures

į.

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TDMA frame **TSN** TS₀ TS₁ transmitted by RN received by Node#A TSN of Rx TS0 of Rx Frame of Rx Frame Marker Frame of Node#A of Node#A Node#A transmitted by TS0 of Tx Frame of TS1 of Tx Frame of Node#A Tx Frame Marker Node#A Node#A of Node#A RxFrameMarker of Node#A, t=TRA

FIG. 61
Time Relationship between various Frame Markers

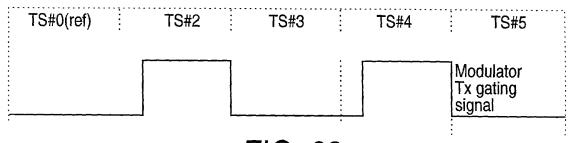
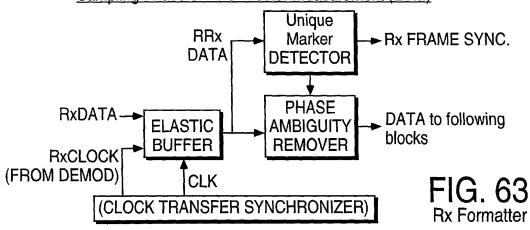


FIG. 62
Tx Frame Gating Signal

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Sampling Phase or Error Vector Measurement (EVM)



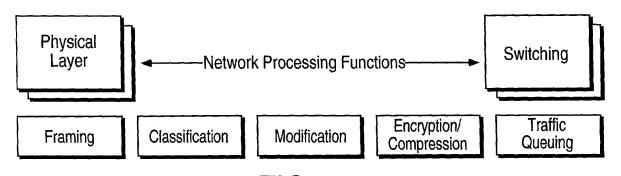


FIG. 64

IP Packet Network Processing Functions

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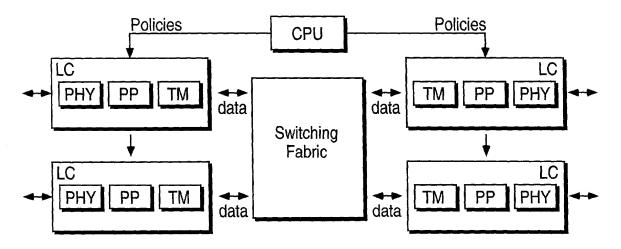


FIG. 65 Distributed Packet Switching Architecture

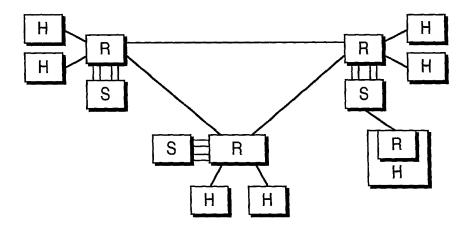


FIG. 66 UniNet Application over Existing Ethernet IP Networks

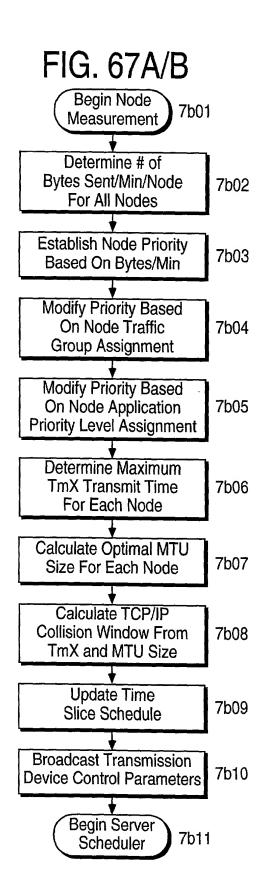
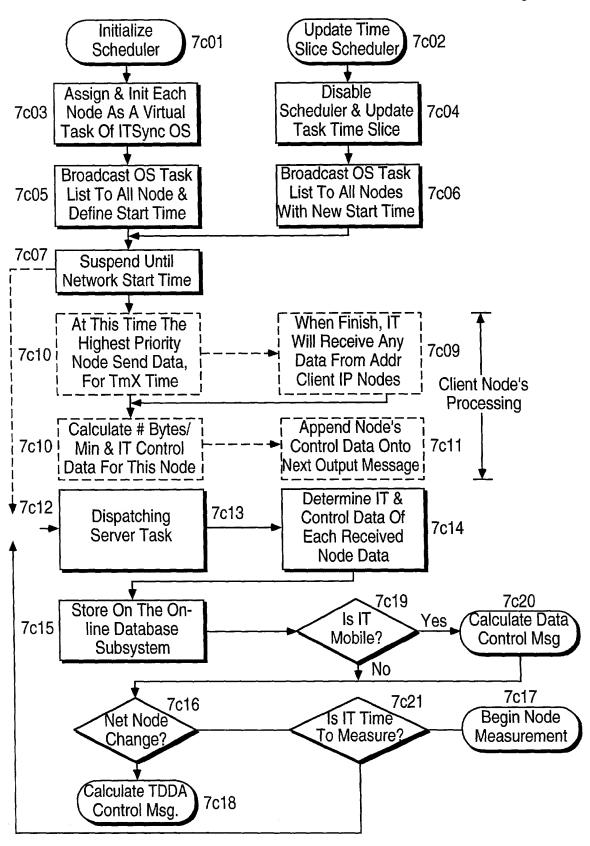


FIG. 67C DIPA/TDDA Algorithm



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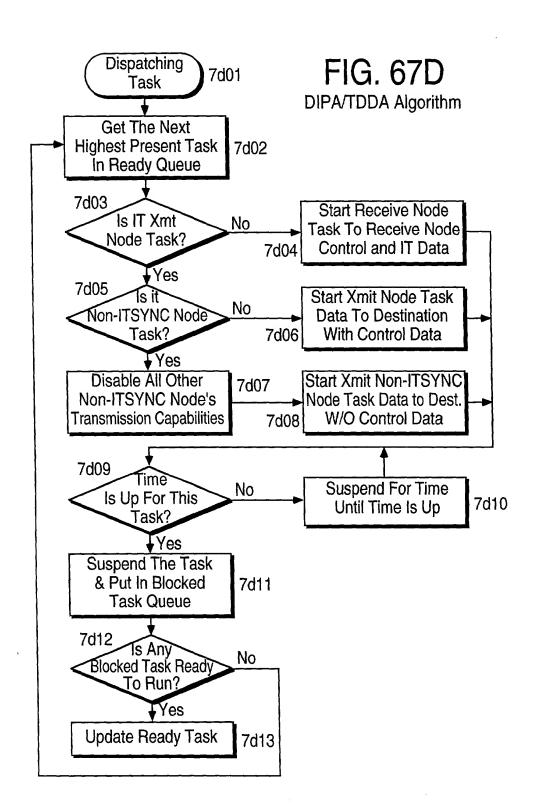
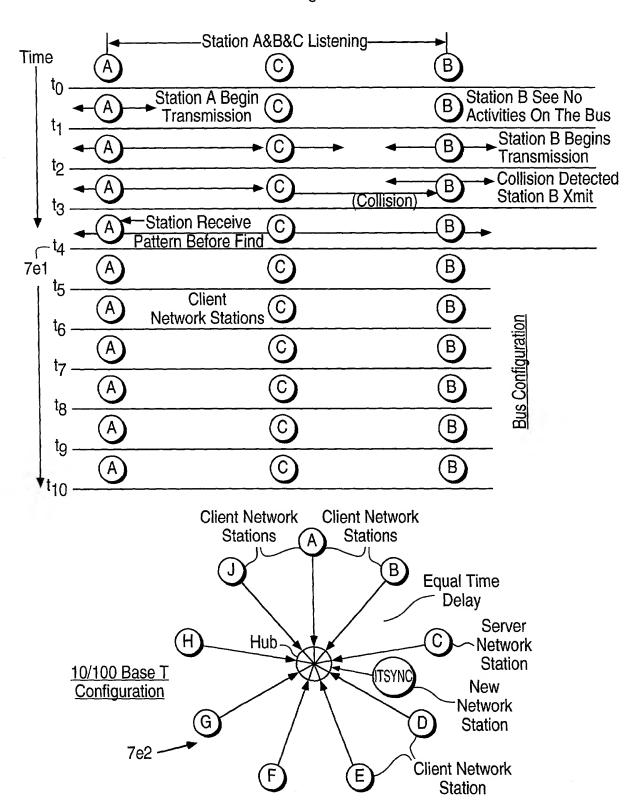
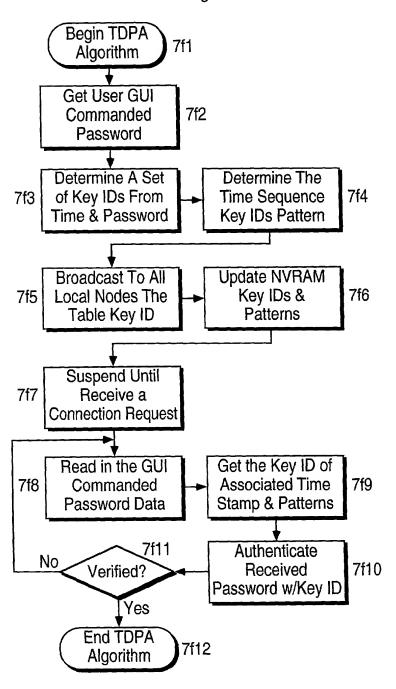


FIG. 67E TDDA Algorithm



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FIG. 67F **TDPA Algorithm**



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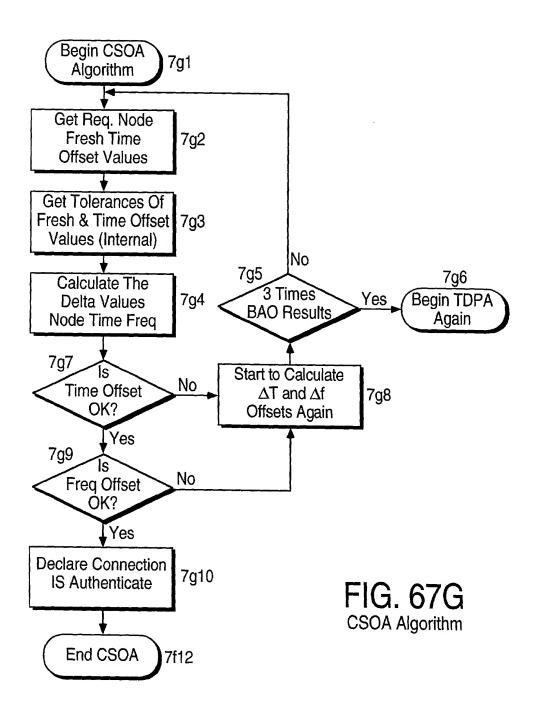
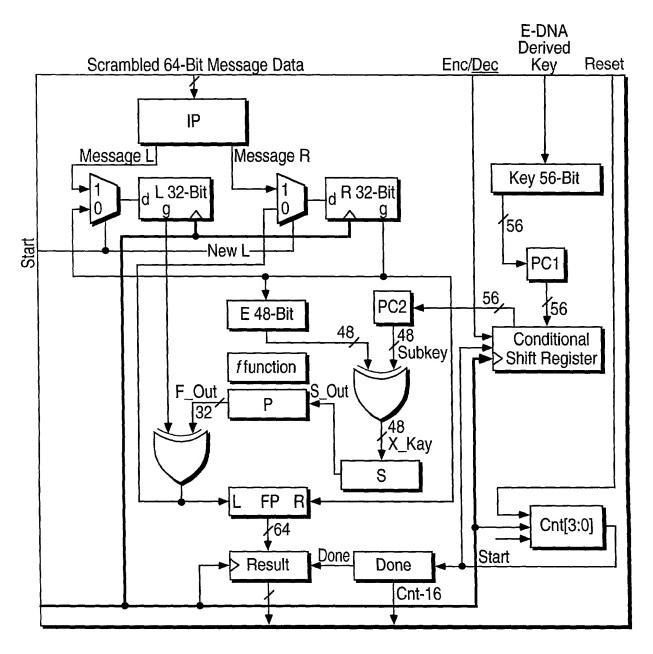


FIG. 67H/I
E-DNA Derived Key with 56 bits DES and Scrambled 64 Data bits



1

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FIG. 67J/K Expected Receiving Parameters Dependent DES Key Generation

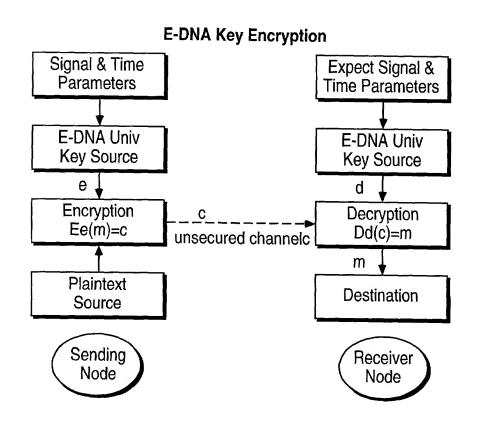
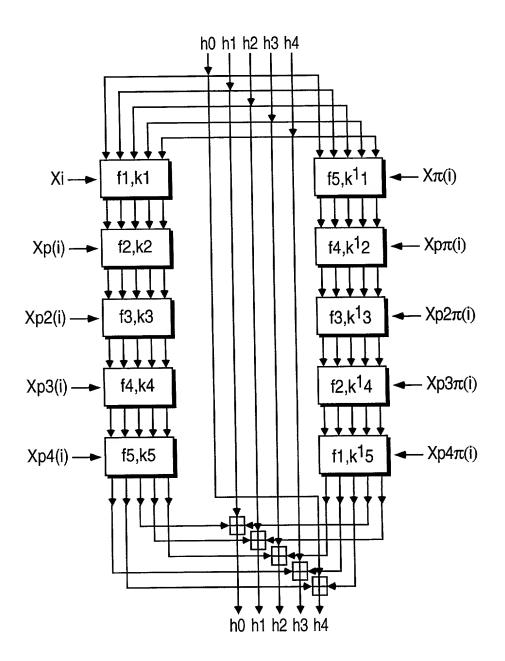


FIG. 67L

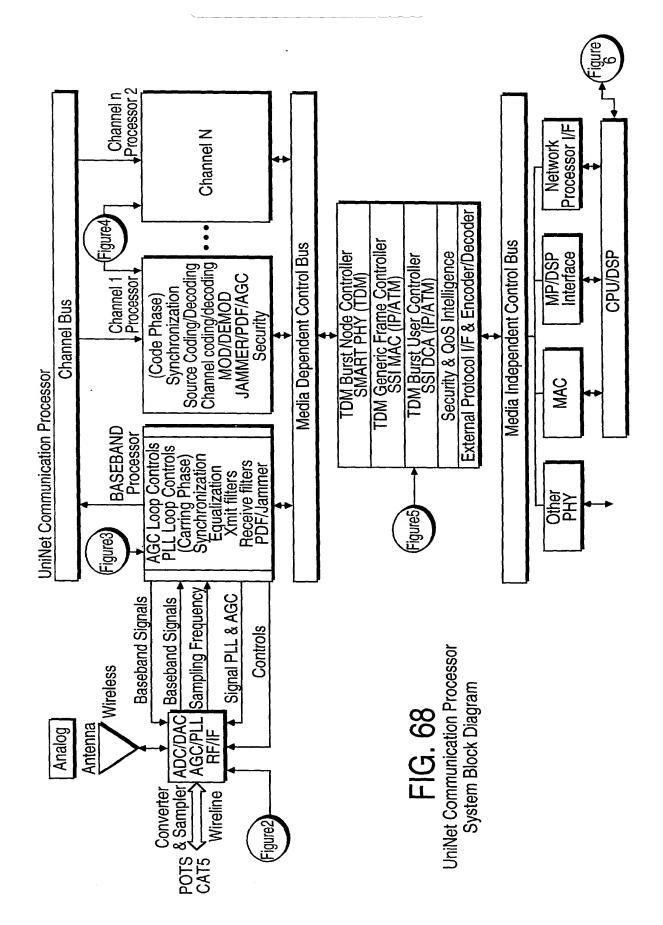
Outline of the compression function of RIPEMD-160. Inputs are a 16 word message block Xi and a 5-word chaining variable h0h1h2h3h4, output is a new value of the chaining variable



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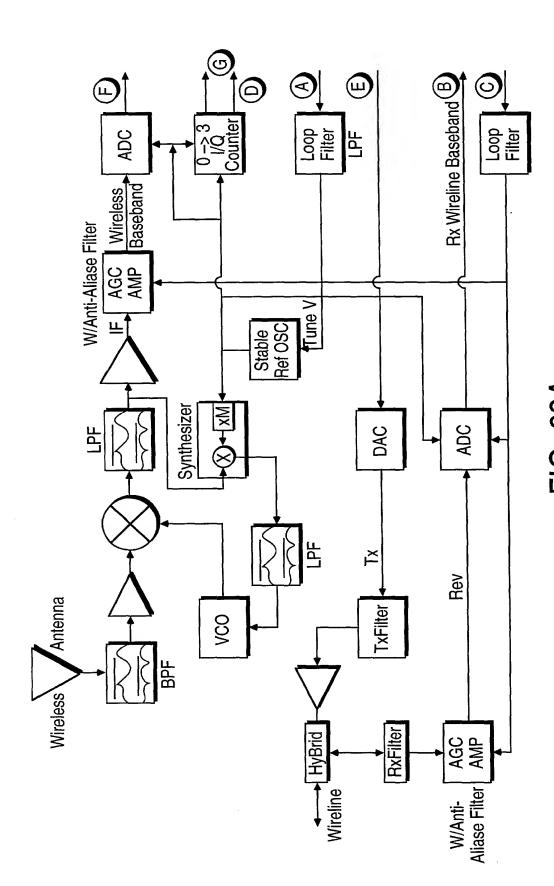


FIG. 69A
Baseband Converter and Sampler (Receiver Only View for Wireless)

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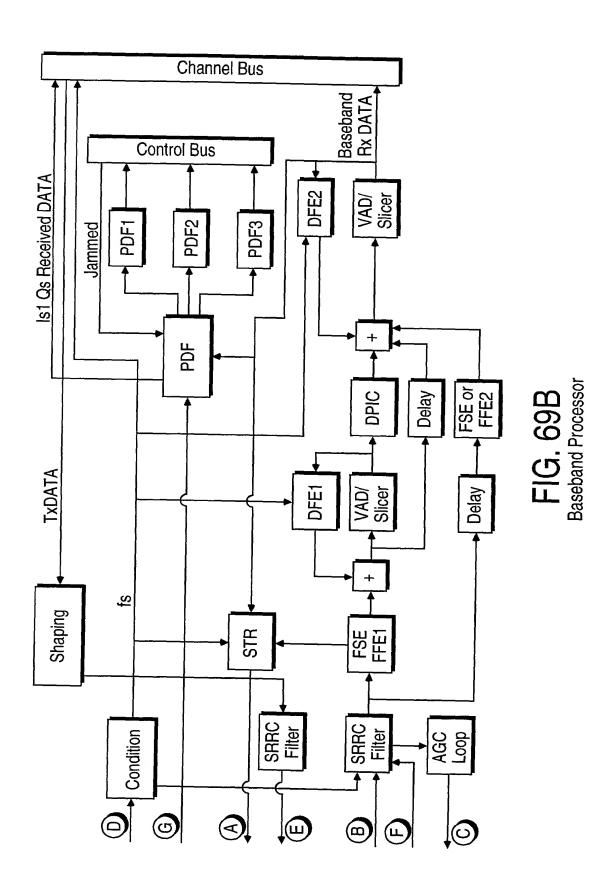
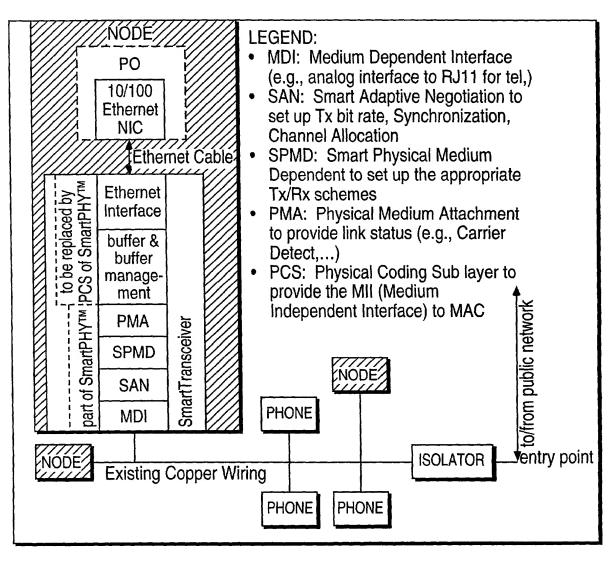
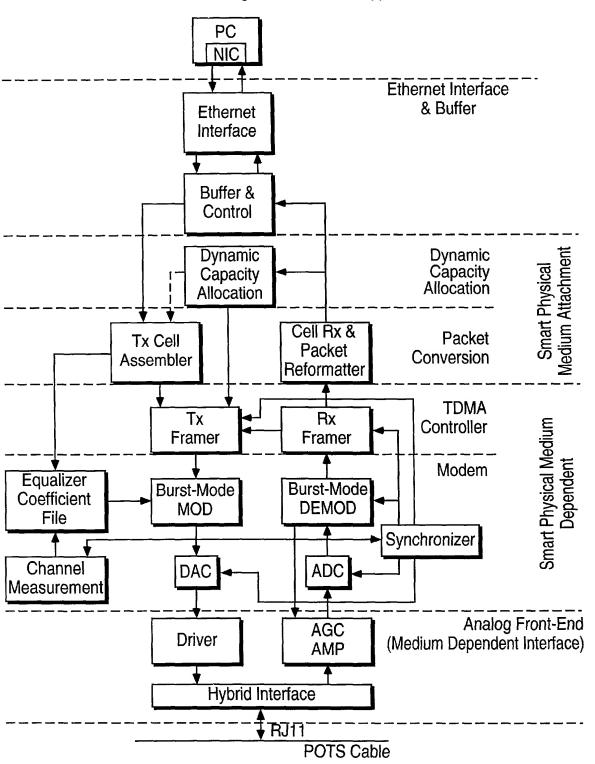


FIG. 70
PoR Prototype System for Applications using POTS as Communications Media



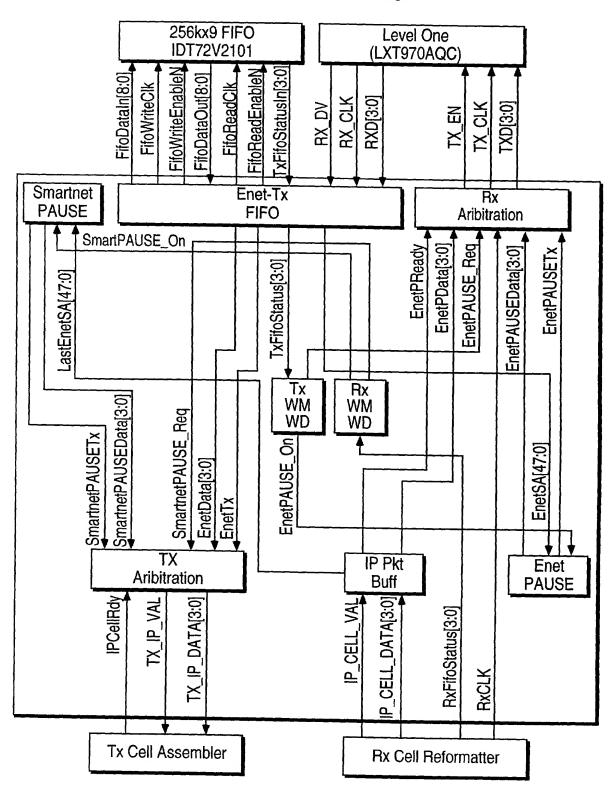
Action of the control of the control

FIG. 71
Block Diagram of the Prototype

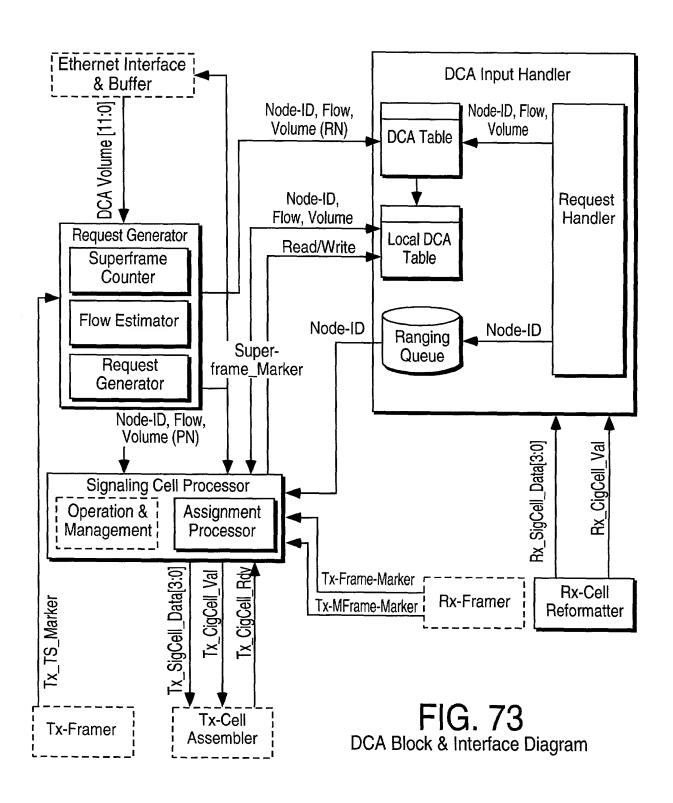


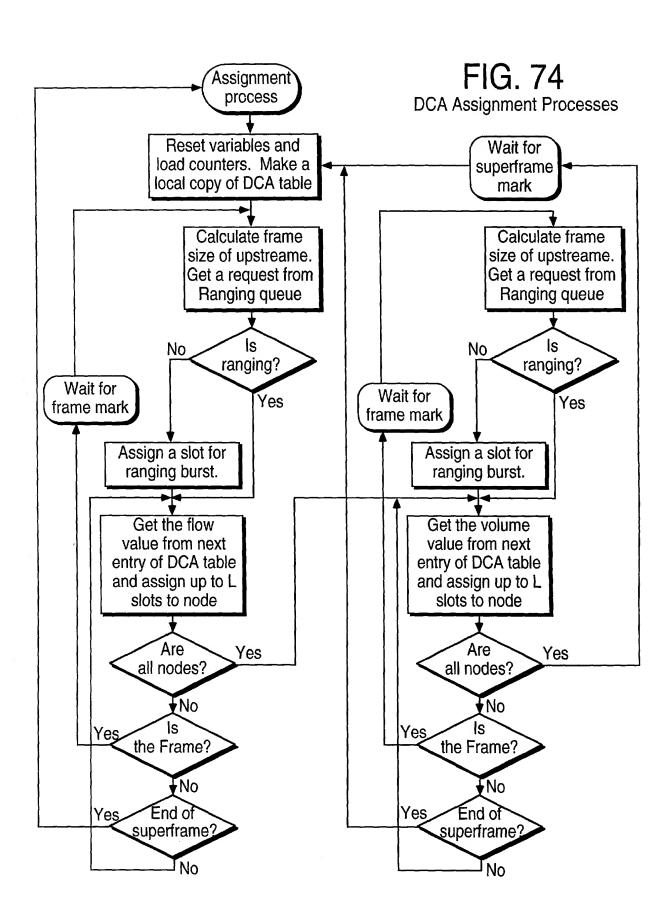
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FIG. 72
Ethernet Interface and Buffer Management



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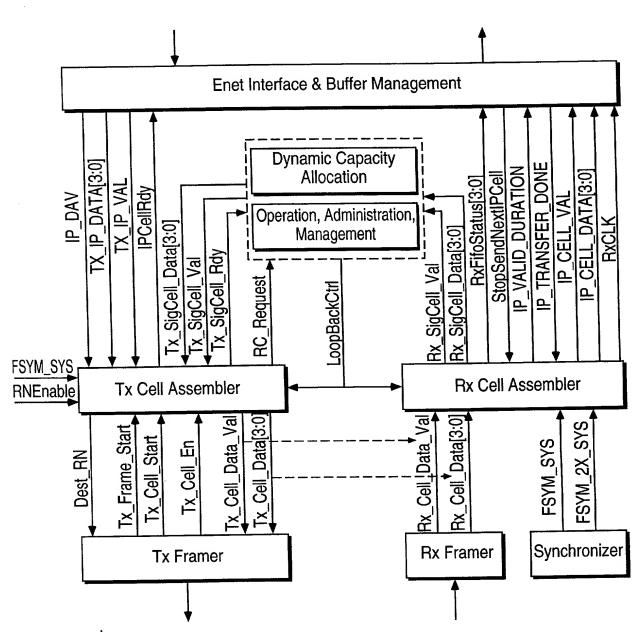
HE H Marty H H

100

14.

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FIG. 75
Packetizer Block Diagram



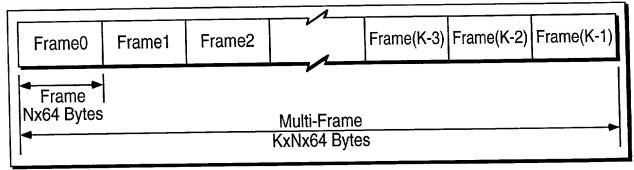


FIG. 76
Multi-Frame Format

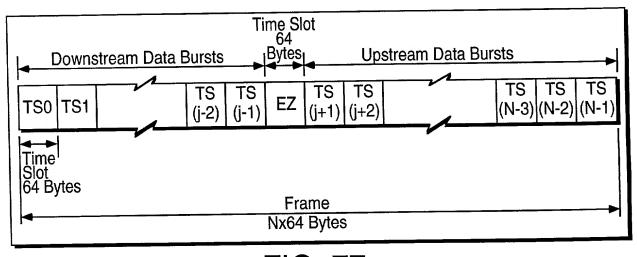


FIG. 77
Frame Format

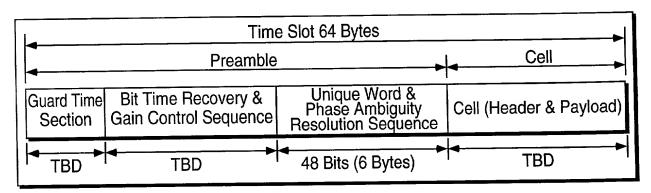


FIG. 78
Burst Format

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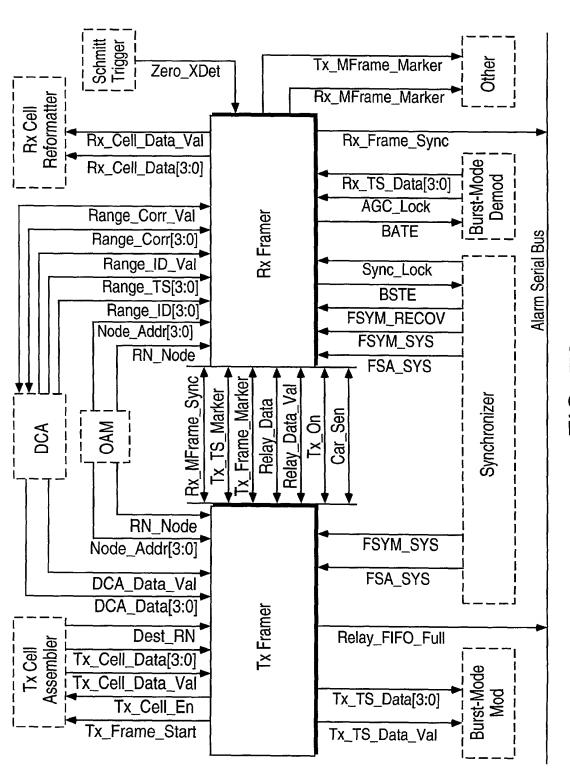


FIG. 79
TDMA Controller Interface

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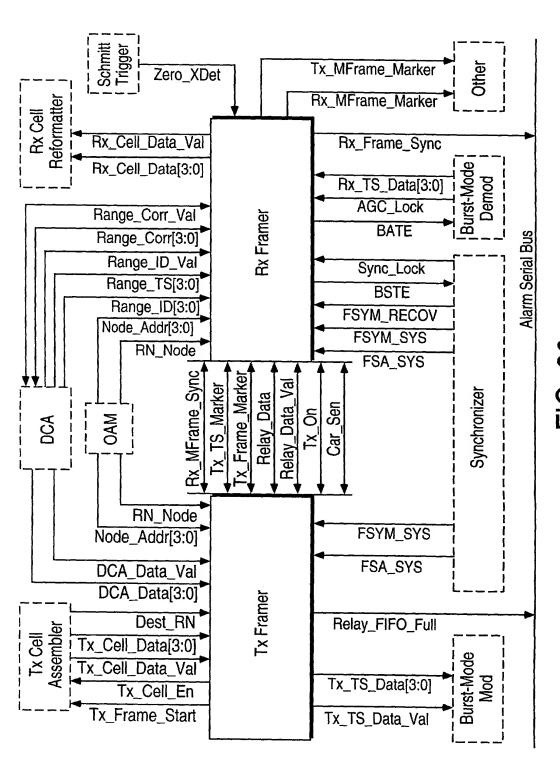
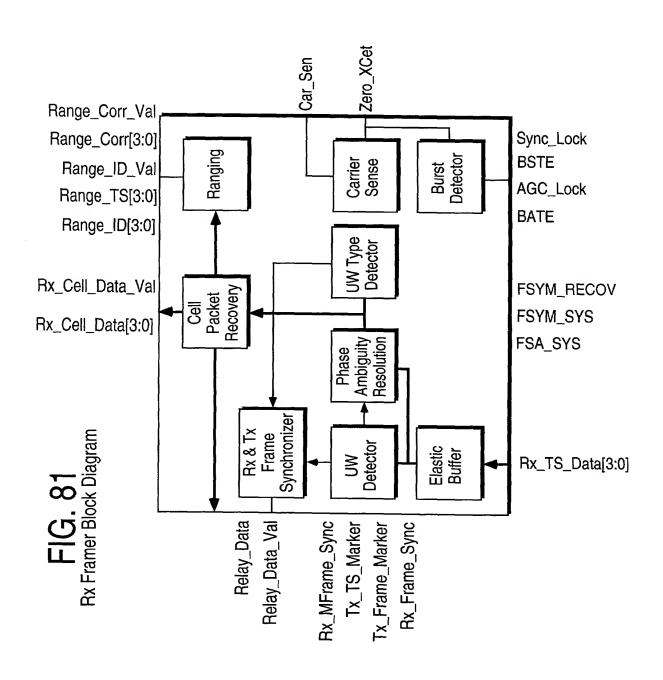
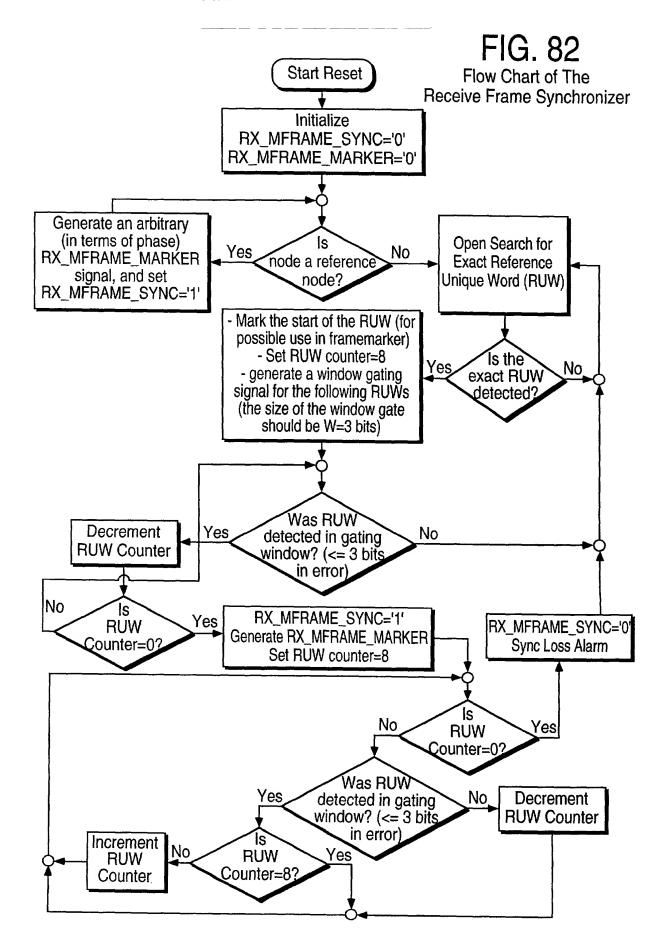


FIG. 80 TDMA Controller Interface

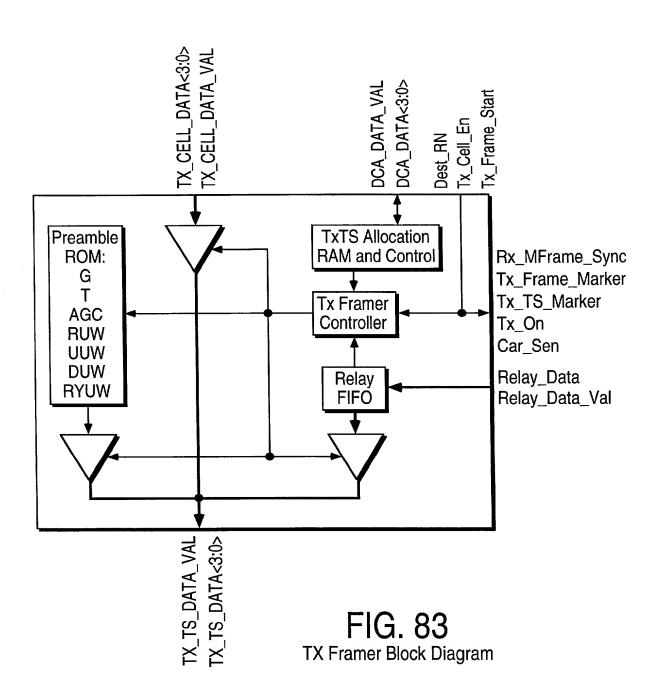


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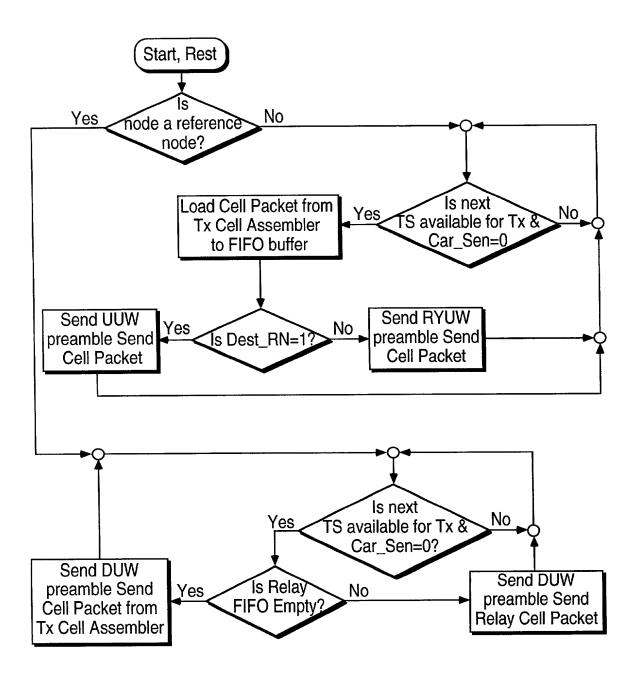


FIG. 84
TX Framer Controller

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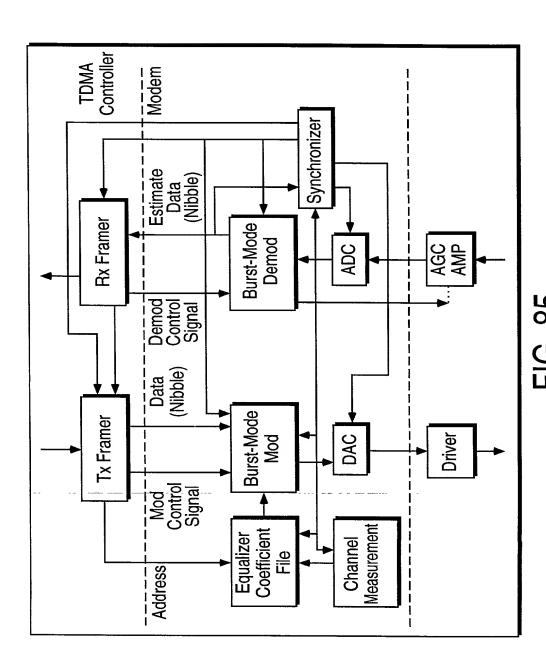
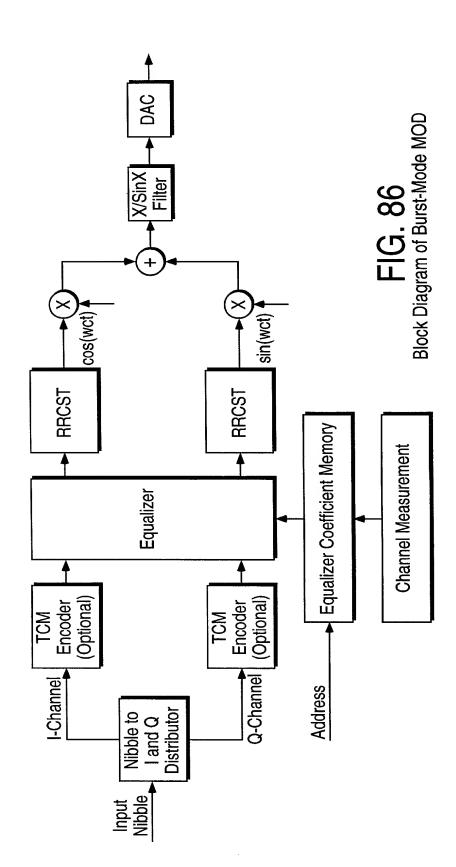


FIG. 85
Burst-Mode Modern Block Diagram

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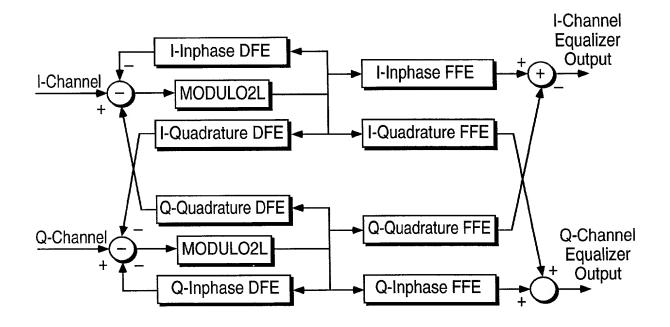


FIG. 87
Block Diagram of Equalizer

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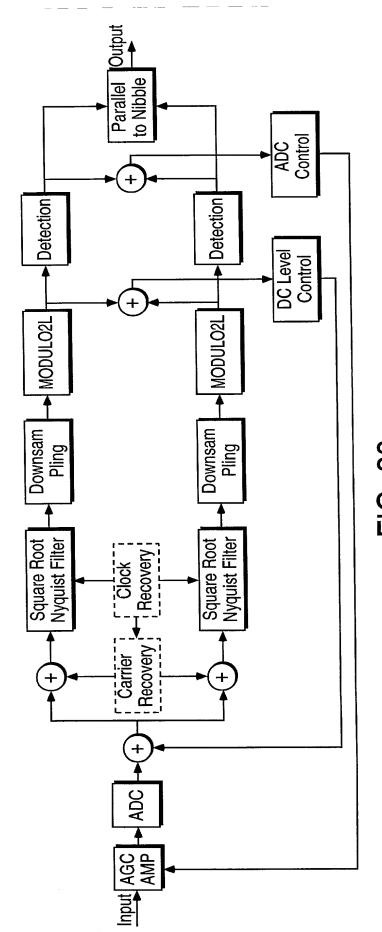


FIG. 88
Block Diagram of Burst-Mode DEMOD

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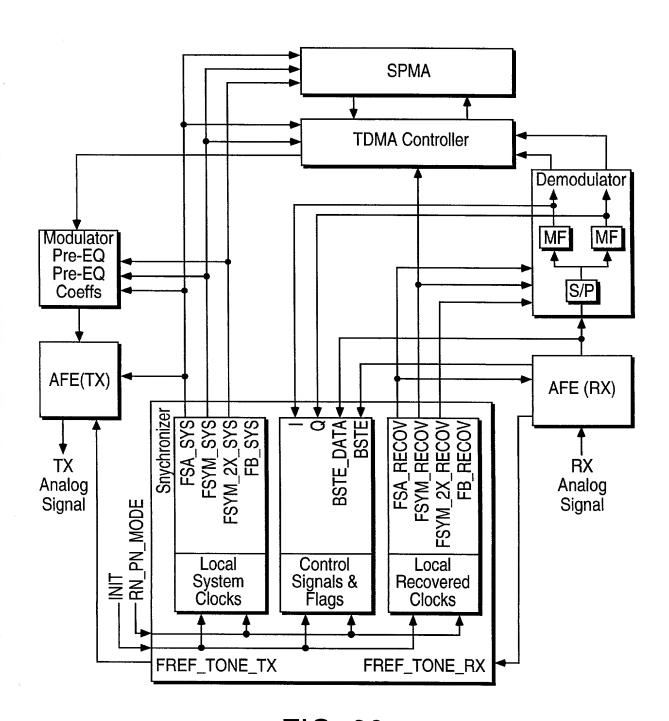


FIG. 89
Synchronizer Block & Interface Diagram

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